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Date 7/22/02 Serial # 09/837,807 Priority Application Date _____

Your Name Mewis Examiner # _____

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The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

02-02 11:47 IN

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-18 (1,2,3,10,11 & 12 are independent claims)

Problem: See Paragraphs 4-10

Solution: " " 11-21

Novelly in structure illustrated in claims

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Searcher: I. SPECKHARD
Searcher Phone: 308-6559
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 7/29/02
Date Completed: 7/29/02
Searcher Prep/Rev Time: 100
Online Time: 150

Type of Search

Structure (#) _____
Bibliographic ✓
Litigation _____
Fulltext ✓
Patent Family _____
Other _____

Vendors

STN ✓
Dialog ✓
Questel/Orbit _____
Lexis-Nexis _____
WWW/Internet _____
Other _____

FILE 'CAPLUS' ENTERED AT 12:36:04 ON 29 JUL 2002

FILE 'HCAPLUS' ENTERED AT 12:36:17 ON 29 JUL 2002

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L14     2176219 S TANTALUM OR TA OR CHROMIUM OR CR OR TITANIUM OR TI OR TUNGSTE
L15        1028 S (WIRING OR WIRE)(3N)LINE
L16         210 S L14 AND L15
L17     2596271 S TANTALUM OR TA OR TITANIUM OR TI OR BARIUM OR BA OR HAFNIUM O
L18      110733 S (INSULAT###### OR DIELECTRIC###)(3N)(LAYER### OR FILM### OR C
L19        8086 S (FIRST OR ONE OR SECOND OR TWO)(3N)(INSULAT###### OR DIELECTR
L20       16758 S L17 AND L8
L21          12 S L20 AND L19
L22      156922 S SEMICONDUCT######(1N)DEVICE
L23      411590 S SEMICONDUCT#####
L24      411590 S L22-L23
L25       13044 S PIXEL
L26         748 S PIXEL  (4N)(MATRIX## OR MATRIC##)
L27        2636 S (MATRIX## OR MATRIC##)(3N)(CIRCUIT OR LOOP OR PATH OR ROUTE O
L28       15361 S L25-L27
L29        2287 S DRIV#(3N)(CIRCUIT  OR LOOP  OR PATH  OR ROUTE OR ELECTRODE)
L30       11559 S TFT OR (THIN()FILM()TRANSISTOR)
L31         521 S (TFT OR (THIN()FILM()TRANSISTOR))(3N)PIXEL
L32       11559 S L30-L31
L33        2439 S LDD OR (LIGHTLY()DOPED()DRAIN)
L34        3989 S N()CHANNEL
L35        3678 S (FIRST OR ONE OR SECOND OR TWO)(3N)(WIRING OR WIRE)
L36          57 S L15 AND L35
L37       63774 S ONO OR OXIDE(2N)SILICON OR OXIDE(2N)NITRIDE OR SILICON(3N)OXI
L38       20028 S IMPURIT###(3N)CONCENTRAT####
L39        6058 S STORAGE(3N)(CAPACIT####### OR CONDENS####)
L40       47568 S LOW##(3N)(POWER OR VOLT OR V OR POTENTIAL)
L41         709 S LOW##(3N)(ELECTRIC##(3N)POTENTIAL)
L42       47606 S L40-L41
L43        1605 S L24 AND L28
L44           5 S L43 AND L20
L45        1600 S L43 NOT L44
L46           4 S L43 AND L16
L47        1596 S L45 NOT L46
L48          45 S L47 AND L29
L49          22 S L48 AND L30
L50          22 S L48 AND L32
L51           8 S L50 AND L33
L52          14 S L50 NOT L51
L53           1 S L52 AND L34
L54          13 S L52 NOT L53
L55        1574 S L47 NOT L50
L56          16 S L55 AND L38
L57           0 S L56 AND L42
L58           0 S L56 AND L39
L59           0 S L56 AND L16
L60          10 S L56 AND L14
L61           6 S L56 NOT L60
L62           0 S L61 AND L20
L63           0 S L61 AND L17
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L64	1558	S	L55 NOT L56
L65	0	S	L64 AND L16
L66	696	S	L64 AND (L14 OR L15)
L67	565	S	L66 AND (L17 OR L18)
L68	558	S	L67 AND L14
L69	497	S	L68 AND L17
L70	190	S	L69 AND L32
L71	8	S	L70 AND L34
L72	182	S	L70 NOT L71
L73	19	S	L72 AND L37
L74	0	S	L73 AND L42
L75	0	S	L73 AND L29
L76	19	S	L73 AND L28
L77	0	S	L73 AND L33
L78	1	S	L73 AND L35
L79	18	S	L76 NOT L78

L44 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:294018 HCAPLUS
DN 136:316725
TI An optoelectronic device having multifunctional **pixels**
IN Underwood, Ian; Gourlay, James
PA Microemissive Displays Limited, UK
SO PCT Int. Appl., 23 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002031882	A1	20020418	WO 2001-GB4505	20011010
	W: JP, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
PRAI	GB 2000-24804	A	20001010		

AB An optoelectronic device is described comprising a **semiconductor** substrate (e.g., Si layer) providing active circuitry, and an array of smart **pixels**, each smart **pixel** comprising part of the active circuitry as well as at least one org. layer which performs at least one of the functions of light detection, light emission, light modulation and light amplification, wherein the smart **pixels** comprise conversion means capable of converting optical signals into elec. signals. A method of fabricating the optoelectronic device is also described.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:610613 HCAPLUS
DN 131:221343
TI Manufacture of array substrates for display devices
IN Dojo, Masayuki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11258633	A2	19990924	JP 1998-63253	19980313

AB Manuf. of the devices comprising a substrate, a scanning line, 1st insulator layer, a **semiconductor** layer, a thin-film transistor comprising source and drain electrodes connected to the **semiconductor** layer, a signal line **lead** from the drain electrode and crossing the scanning line in near right angle, and **pixel** electrodes elec. connected to the source electrode is claimed. The manufg. process includes (A) formation of a scanning line having Al alloy/high m.p. metal laminate structure, (B) formation of the gate insulator directly contacting the scanning line and the gate electrode at substrate temp. .gtoreq.300.degree., and (C) formation of **pixel** electrode, laminated on gate insulator, by dry etching. Damaging of Al alloy scanning line during etching is prevented by formation of high m.p. metal and gate insulator layers thereon.

L44 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:610612 HCAPLUS
DN 131:221342
TI Array substrates for display devices
IN Dojo, Masayuki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11258632	A2	19990924	JP 1998-63251	19980313

AB The array substrate consists of a substrate, a scanning line, 1st insulator layer, a **semiconductor** layer, a thin-film transistor comprising source and drain electrodes connected to the **semiconductor** layer, a signal line **lead** from the drain electrode and crossing the scanning line in near right angle, and **pixel** electrodes elec. connected to the source electrode, and the scanning line has a multilayer structure of Al alloy and high-m.p. metal and the gate insulator directly connected to the scanning line and the gate electrode comprises a film formed under substrate temp. of .gtoreq.300.degree.. The resistance of the scanning line is decreased and incomplete interlayer insulation is prevented.

L44 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:483259 HCAPLUS
DN 127:103117
TI Thin-film electron emission sources and display devices using thereof
IN Suzuki, Mutsuzo; Kusunoki, Toshiaki
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09139175	A2	19970527	JP 1995-296471	19951115

AB The electrode for the emission sources comprises an upper and lower electrodes. The upper electrode is a double-layer electrode whose layer (1) adjacent to an insulator film is made of **Ti**, V, Rh, Pt, **Th**, Zr, **Hf**, Ru, Mo, Ir, Nb, **Ta**, Re, Os, and/or **W** in prevention of electromigration and (2) exposed to a vacuum space is made of Au, Ag, Cu, and/or Al for surface stability. The lower electrode is made of a **semiconductor**. The metal electrode components give the display devices stable **pixels** and picture.

L46 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:781339 HCAPLUS
DN 135:337816
TI Contact structures of wirings and methods for manufacturing the same, and thin film transistor array panels including the same and methods for manufacturing the same
IN Kong, Hyang-shik; Hur, Myung-koo; Kim, Chi-woo
PA S. Korea
SO U.S. Pat. Appl. Publ., 41 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001032981	A1	20011025	US 2001-837374	20010419
JP 2001358343	A2	20011226	JP 2001-109577	20010409
PRAI KR 2000-20807	A	20000419		

AB First, a conductive material of aluminum-based material is deposited and patterned to form a gate **wire** including a gate **line**, a gate pad, and a gate electrode. A gate insulating layer is formed by depositing nitride **silicon** in the range of >300.degree.. for 5 min, and a **semiconductor** layer an ohmic contact layer are sequentially formed. Next, a conductor layer of a metal such as **Cr** is deposited and patterned to form a data **wire** include a data **line** intersecting the gate line, a source electrode, a drain electrode and a data pad. Then, a passivation layer is deposited and patterned to form contact holes exposing the drain electrode, the gate pad and the data pad. Next, indium zinc oxide is deposited and patterned to form a **pixel** electrode, a redundant gate pad and a redundant data pad resp. connected to the drain electrode, the gate pad and the data pad.

L46 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:658013 HCAPLUS
DN 135:203115
TI Contact structure of wiring and a inexpensive method for manufacturing the same for TFT flat panel displays
IN You, Chun-gi
PA S. Korea
SO U.S. Pat. Appl. Publ., 49 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001019129	A1	20010906	US 2001-755193	20010108
	JP 2001267420	A2	20010928	JP 2001-1118	20010109
PRAI	KR 2000-712	A	20000107		
	KR 2000-27126	A	20000519		
	KR 2000-57037	A	20000928		

AB First, a conductive material made of Al-based material is deposited and patterned to form a gate **wire** including a gate **line**, a gate pad, and a gate electrode. A gate insulating layer is formed, and a **semiconductor** layer and an ohmic contact layer are sequentially formed. Next, a conductor layer including a lower layer of **Cr** and an upper layer of Al-based material is deposited and patterned to form a data **wire** include a data **line** intersecting the gate line, a source electrode, a drain electrode and a data pad. Then, a passivation layer is deposited and a thermal treatment process using annealing step is executed. At this time, all or part of Al oxide (AlOx) layer having a high resistivity, which is formed on the gate wire and/or the data wire during manufg. process, may be removed. Then, the passivation layer is patterned to form contact holes exposing the drain electrode, the gate pad and the data pad, resp. Next, IZO is deposited and patterned to form a **pixel** electrode, a redundant gate pad and a redundant data pad resp. connected to the drain electrode, the gate pad and the data pad, resp. By removing Al oxide (AlOx) layer having a high resistivity, through annealing step, the contact resistance between the metal of Al-based material, and IZO may be minimized, because they directly contact each other.

L46 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:341850 HCAPLUS
DN 126:324273
TI **Semiconductor** or liquid-crystal device, an active-matrix substrate, and their production
IN Fukumoto, Yoshihiko
PA Canon K. K., Japan
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 768710	A2	19970416	EP 1996-306683	19960913
	EP 768710	A3	19970730		
	R: DE, FR, GB, IT, NL				
	JP 09148329	A2	19970606	JP 1996-241939	19960912
PRAI	JP 1995-236865	A	19950914		
	JP 1996-241939	A	19960912		

AB The prodn. of a **semiconductor device** comprises polishing a region of an elec. conductive material serving as an electrode or a **wiring line** in an insulating layer formed on a **semiconductor** region, the region of elec. conductive material being elec. connected to the **semiconductor** region, where a region of another material is formed within the elec. conductive material to be polished. The prodn. of an active-**matrix** substrate comprises polishing metal **pixel** electrodes provided at intersections of multiple signal lines and multiple scanning lines and a means for applying voltage to the **pixels**, where a region of another material is formed within the **pixel** electrode to be polished.

L46 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:30148 HCAPLUS
DN 118:30148
TI Thin film-transistor array substrate for active matrix display device and its manufacture
IN Minamino, Yutaka; Takeda, Yoshiya; Imada, Tatsuo
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04140725	A2	19920514	JP 1990-263996	19901001

AB A thin film-transistor array substrate comprises (1) gate bus **lines** and first electrode **wirings** alternatively formed by first transparent conducting films on an insulating transparent substrate, (2) gate electrodes formed by first metal films at the part of the gate bus lines, (3) insulating films formed by covering the gate bus lines, gate electrodes, and primary electrode wiring, (4) **semiconductor** layers formed on the gate electrodes through the insulating films, (5) source bus lines crossing the gate bus lines and **pixel** electrodes formed by second transparent conducting films covering the first electrode wiring, (6) source and drain electrodes formed by second metal films on the **semiconductor** layers and also covering the source bus lines, wherein the source electrodes are connected to the source bus lines, the drain electrodes to the **pixel** electrodes, and capacitors are formed by the first electrode wirings, the insulating films, and the **pixel** electrodes. An addnl. thin film-transistor array substrate with some modifications, e.g. gate electrodes formed by a metal film on the gate bus lines except the area forming capacitors, is described. It is manufd. in multisteps by forming sequentially each component on an insulating substrate. The double layer structure of the transparent electrode and the metal film for the gate and source bus lines provides a capacitor with a large capacitance with out lowering the opening ratio and also gives redundancy to the bus lines.

L51 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:194138 HCAPLUS
TI **Semiconductor device** and its production method. [Machine Translation].
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 23 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002076351	A2	20020315	JP 2000-259895	20000829

AB [Machine Translation of Descriptors]. Until recently, when the formation tries to do the **TFT** which has **LDD** structure and the **TFT** which has GOLD structure, it becomes something where the manufacturing process is complicated and there was a problem where the number of processes increases. This invention makes the **TFT** which uses p channel type TF T155 where the off electric current is low for **pixel** section 150 produces with 5 photomasks N channel type TF T153 which has GOLD structure, with 154 as the **TFT** of **drive circuit** 1

L51 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:139209 HCAPLUS
TI Thin film **semiconductor device**. [Machine Translation].
IN Kunii, Masafumi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002057339	A2	20020222	JP 2000-241984	20000810
	US 2002068372	A1	20020606	US 2001-921532	20010803
PRAI	JP 2000-241984	A	20000810		

AB [Machine Translation of Descriptors]. Integrating the **thin film transistor** for **drive** possible **circuit** and the **thin film transistor** for the **pixel** where the leak elec. current is small on the identical baseplate at low voltage, offers the thin film **semiconductor device** which is suited for low spending elec. drive and high quality picture indication. The **pixel** array section of the thin film **semiconductor device** **pixel** electrode 11 and this the switching includes with the **thin film transistor** **TFT**-PXL for the **pixel** which is driven, the peripheral **circuit** includes the **drive circuit** which is formed in order to drive the **thin film transistor** for the **pixel** with **thin film transistor** **TFT**-CKT for circuit. Each **thin film** **transistor**, **semiconductor** thin film 5 and gate electrode 1 and, the gate insulator has the laminate structure which repeats with 2 which lies between at these time and 3. **Semiconductor** thin film 5 has with channel territory ch and follow the surrounding of the channel territory low d. impurity territory **ldd** and high d. impurity territory s/d which follows the surrounding of the low d. impurity territory and separates the low d. impurity territory and the high d. impurity territory the d. boundary B which are located inside from end E of gate electrode 1. As for site X of the d. boundary B which measured the end E of the gate electrode in std., the **TFT**-CKT, the **TFT**-PXL compared to, is set inside.

L51 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:281313 HCAPLUS
TI Production method of **thin film transistor** device. [Machine Translation].
IN Seto, Shunsuke
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001111054	A2	20010420	JP 1999-284189	19991005

AB [Machine Translation of Descriptors]. With the active **matrix** baseplate of **drive circuit** one type, the wiring malfunction due to the pattern defectiveness of the gate metal membrane is prevented, the liquid crystal display of high indicatory grade is made production possible at high yield rate. The gate metal membrane which forms a membrane on gate insulator 30, gate line (not to illustrate), in gate electrode 32, 33 and 34 after the pattern formation, gate electrode 32, 33 and 34 or resist mask 71 - 76 in the mask to do necessary ion doping in each **semiconductor** layer 26, 27 and 28 with 1 photolithography process, the formation to do n-**ldd** territory 26 B, 26 C, 28 B, 28 C, and source territory 26 D, 28 D and drain territory 26 E and 28 E in N type **semiconductor** layer 26 and 28, in p type **semiconductor** layer 27 source territory 27 B and Drain territory 27 C the formation is done.

L51 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:211112 HCAPLUS
TI **Semiconductor device** and its production method. [Machine Translation].
IN Yamazaki, Shunpei; Arai, Yasuyuki; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 26 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001077374	A2	20010323	JP 2000-204291	20000705
PRAI JP 1999-191097	A	19990706		

AB [Machine Translation of Descriptors]. The manufacturing process becomes complicated ones in order to produce the **TFT** which corresponds to various **circuits** of the active **matrix** baseplate the number of processes increases. Increase of the number of processes not only becoming the increase primary factor of production cost, becomes the cause of decreasing production yield rate. P channel type **TFT** of **drive circuit** makes single drain structure, N channel type **TFT** that does which of GOLD structure and **LDD** structure. The denseness touching on the protective insulator film and the said insulator film which consist of the inorganic insulating material ingredient where as for **pixel TFT** the **pixel** electrode which is provided in the **pixel** section as **LDD** structure, the formation is done on the insulator film between the layer which consists of the organic insulator ingredient at least, provides in the upper part of the gate electrode of **pixel TFT** through the opening hole which in the insulator film between the said layer which was formed is provided, is connected to aforementioned **pixel TFT**. The number of photomasks is designated as 6 - 8 in this process.

L51 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:185464 HCAPLUS
TI **Semiconductor device** and its production method. [Machine Translation].
IN Kitakado, Hideto; Kawasaki, Ritsuko; Kasahara, Kenji
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 22 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001068680	A2	20010316	JP 2000-101787	20000404
	US 6346730	B1	20020212	US 2000-541608	20000403
	US 2002058364	A1	20020516	US 2002-35205	20020104
PRAI	JP 1999-99481	A	19990406		
	JP 1999-176120	A	19990622		
	US 2000-541608	A3	20000403		

AB [Machine Translation of Descriptors]. The performance characteristic of the **semiconductor device** and that improves reliability are designated as purpose by making appropriate ones structure of the **TFT** of bottom gate type or the opposite stagger type which is arranged in each circuit of the **semiconductor device**, according to the function of circuit. **LDD** territory 159 of N channel type TF T169 of **pixel TFT** - 162 is not piled up with the channel protective insulator film, at the same time, in order for part to be piled up with the gate electrode at least, arranges, **LDD** territory 153,154 of N channel type TF T168 of **drive circuit** is not piled up with the channel protective insulator film, at the same time, in order for part to be piled up with the gate electrode at least, is arranged, **LDD** territory 148,149 of p channel type TF T167 of **drive circuit** is piled up with the channel protective insulator film, at the same time, in order to be piled up with the gate electrode, arranges.

L51 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:888279 HCAPLUS
TI Electro-optic device and its production method. [Machine Translation].
IN Ikeda, Takayuki; Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 24 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000353811	A2	20001219	JP 2000-100257	20000403
PRAI	JP 1999-99683	A	19990407		

AB [Machine Translation of Descriptors]. The **TFT** of appropriate structure is arranged according to circuit function, the **semiconductor device** which possesses high reliability is offered. Gate insulator 115,116 of drive **TFT** is designed thinner than gate insulator 117 of **pixel TFT** in the **semiconductor device** which possesses with the **drive circuit** and the **pixel** section on the identical nonconductor. In addition, with **pixel TFT** channel formation territory 112 A and 112 B the formation are done under gate electrode 121, separation territory 113 is formed between that. At that occasion, **LDD** territory 111 A and 111 D have with the territory which is not piled up with the territory which is piled up to the gate electrode.

L51 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:880888 HCAPLUS
TI **Semiconductor device** and its production method. [Machine Translation].
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 24 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000349299	A2	20001215	JP 2000-85444	20000324
	US 6399988	B1	20020604	US 2000-533040	20000322
PRAI	JP 1999-84997	A	19990326		

AB [Machine Translation of Descriptors]. The performance characteristic of the **semiconductor device** and that improves reliability are designated as purpose by making appropriate ones structure of the **TFT** which is arranged in each circuit of the **semiconductor device**, according to the function of circuit. The **LDD** territory of N channel type **TFT** of the aforementioned **pixel** section, in order not to be piled up with the gate electrode of said **pixel TFT**, to be arranged in the **semiconductor device** which possesses with the **drive circuit** of the **pixel** section and the said **pixel** section on the identical baseplate, the **LDD** territory of 1st N channel type **TFT** of aforementioned **drive circuit** to be arranged, in order to be piled up with the gate electrode of said 1st N channel type **TFT**, the **LDD** territory of 2nd N channel type **TFT** of aforementioned **drive circuit** to be arranged, in order the gate electrode of said 2nd N channel type **TFT** and, for part to be piled up at least, aforementioned **pixel TFT** It designates that the offset territory is formed as feature with the channel formation territory and the **LDD** territory of aforementioned **pixel TFT**.

L51 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:579971 HCAPLUS
DN 129:253416
TI **Thin-film transistors** and their manufacture, and liquid-crystal displays using them
IN Seto, Toshihiro
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10233511	A2	19980902	JP 1997-37805	19970221

AB The process comprises sequential formation of polysilicon, gate insulator, and lower and upper gate metal films on an insulating substrate, patterning the lower and upper gate metal films to normal and inverse tapered cross sections, forming a double-layer gate wiring layer (e.g., from a Mo alloy) over the channel region, and simultaneous formation of the source-drain and **lightly doped drain** regions by ion implantation using the gate metal layer as a mask. The liq. crystal display has an array substrate having **pixel electrodes** arranged in a **matrix** and the **thin-film transistors** to **drive** the **pixel electrodes** on an insulating substrate, an opposite electrode substrate, and a liq.-crystal compn. sealed between the substrates. Deviation of the lengths of the **lightly doped drain** regions is minimized.

L53 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:838001 HCAPLUS
TI Production method of **semiconductor device**. [Machine Translation].
IN Yamazaki, Shunpei; Koyama, Jun; Kitakado, Hideto
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 47 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000332256	A2	20001130	JP 2000-66044	20000310
	US 6306694	B1	20011023	US 2000-523675	20000310
	US 2002028543	A1	20020307	US 2001-972859	20011010
PRAI	JP 1999-65737	A	19990312		
	US 2000-523675	A3	20000310		

AB [Machine Translation of Descriptors]. The operational performance and the **semiconductor device** and its production method reliability being high are offered. Lov territory 207 is arranged in **N channel** type TF T302 which forms the **drive circuit**, the **Tft** structure which is strong in the degradation with hot carrier injection is actualized. In addition, Loff territory 217 - 220 is arranged in **N channel** type **TFT** 304 which forms the **pixel** section, **Tft** structure of low off electric current value is actualized. Because the whole is activated sufficiently by optical annealing, the satisfactory bonding section the formation it does the N type impurity territory (B) where this time, in the Lov territory the N type impurity element exists at the density which is higher than the Loff territory, becomes the Lov territory with the channel formation territory.

L54 ANSWER 1 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:332456 HCAPLUS
DN 136:332911
TI polycryst. silicon **thin-film transistor** liquid crystal display
IN Nanno, Yutaka; Senda, Kouji; Takehashi, Shin-Itsu
PA Matsushita Electric Industrial Co., Ltd., Japan
SO PCT Int. Appl., 63 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2002035507	A1	20020502	WO 2001-JP9489	20011029
W: CN, KR, SG, US				
PRAI JP 2000-328716	A	20001027		
JP 2000-384840	A	20001219		

AB The invention relates to a display app., comprising a liq. crystal section wherein unit **pixels** having **pixel** switching elements and **pixel** electrodes are arranged in a matrix form, a scanning side **drive circuit**, a signal side **drive circuit**, and a power source circuit. The **pixel** switching element is a **thin-film transistor** constituted of a polycryst. silicon **semiconductor** formed on an insulating substrate. The power source circuit is a charge-pump system power source circuit, which is a built-in circuit constituted of a polycryst. silicon **semiconductor** and formed integrally on the insulating substrate. This constitution provides a liq. crystal display which enables a marked redn. in power consumption.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L54 ANSWER 2 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:848352 HCAPLUS
TI Nonvolatile memory and **semiconductor device**. [Machine Translation].
IN Kato, Kiyoshi; Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 27 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001326289	A2	20011122	JP 2001-63434	20010307
PRAI	JP 2000-64223	A	20000308		

AB [Machine Translation of Descriptors]. The **semiconductor device** which the nonvolatile memory, make high / multi-functionality and miniaturization possible the nonvolatile memory and the nonvolatile memory which make low power source voltage conversion and low spending electrical conversion possible ingredient preparation is done is offered. Constitutes the memory cell array which is formed the nonvolatile memory by memory **TFT** (**thin film transistor**) of complete empty R type, by the **drive circuit** and other peripheral circuit of the memory cell, these the formation makes just on the identical baseplate. In addition **drive circuit** and the nonvolatile memory which drive the **pixel** section and the **pixel** section which form the **semiconductor device**, the formation it makes just on the baseplate which possesses the insulated surface. Low power source voltage conversion, low spending electrical conversion and rewriting frequency improvement of the nonvolatile memory become possible by using memory **TFT** of complete empty R type. High / multi-functionality and miniaturization of the nonvolatile memory and the **semiconductor device** are actualized by the formation making circuit and the **semiconductor** part which are formed by the **TFT** just.

L54 ANSWER 3 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:796963 HCAPLUS
TI **Semiconductor** display and its driving method. [Machine Translation].
IN Osamu, Mitsuaki; Tanaka, Yukio
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 28 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001306041	A2	20011102	JP 2001-20110	20010129
PRAI JP 2000-24471	A	20000201		

AB [Machine Translation of Descriptors]. The occasion where opposition common reversal drive is done with the active matrix type **semiconductor** display, gate bias as former reversal drive evading the sudden rise range of the OFF electric current by the fact that makes the same extent, hold down the leak of the retention electric charge, at the same time guarantee the ON & the OFF margin of **pixel TFT**. And in **pixel TFT** guarantees gate resisting pressure by the fact that the gate bias which sign yes is done is maintained near former voltage, it designates that the new **drive circuit** which can actualize circuit the low spending electrical conversion of altogether drive is offered as purpose. As for the **semiconductor** display of this invention, while guaranteeing the ON & the OFF margin of **pixel TFT** in gate signal line side **drive circuit** by giving the buffer electric potential which differs from with the frame where the opposition common electric potential takes the + side electric potential making use of the tristate buffer, and - the frame which takes the side electric potential, it is possible to make the voltage amplitude at the time of opposition common reversal drive small.

L54 ANSWER 4 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:692641 HCAPLUS
TI **Semiconductor device** and its production method. [Machine Translation].
IN Yamazaki, Shunpei; Koyama, Jun; Arai, Yasuyuki; Kuwahara, Hideaki
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 34 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001255560	A2	20010921	JP 2000-69563	20000313

AB [Machine Translation of Descriptors]. Reducing the number of processes which produce **pixel TFT**, decrease of production cost and improvement of yield rate in the large area baseplate of the actualization sushi and with the **TFT** which satisfies the quality which each circuit requires the glass substrates et cetera the formation doing the **drive circuit** which the formation does in the lumping together, offers the display which mounts **drive circuit**, it designates that the technology which improves reliability and productivity is offered as theme. In the **pixel** territory **pixel TFT** which the formation is done with opposite stagger type **TFT** of channel etching type the formation is done on the 1st baseplate, patterning of the source territory and the drain territory and patterning of the **pixel** electrode are done with the same photomask. In **drive circuit** and the said **drive circuit** which are formed making use of the **TFT** possessing the crystalline **semiconductor** layer the plural formations it does those which designate the input/output terminal which the subordination is done as one unit, on the 3rd baseplate, after that resolves the 3rd baseplate every individual unit and it designates that the stick driver which can, is mounted on the 1st baseplate as feature.

L54 ANSWER 5 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:376877 HCAPLUS
DN 134:359595
TI Liquid crystal display device having improved **thin film transistors** and a fabrication method thereof
IN Miyazawa, Toshio; Mimura, Akio
PA Hitachi, Ltd., Japan
SO Eur. Pat. Appl., 32 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1102111	A2	20010523	EP 2000-124340	20001117
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001147446	A2	20010529	JP 1999-329725	19991119
PRAI	JP 1999-329725	A	19991119		

AB A liq. crystal display device is provided with a **pixel** area on a substrate having plural gate lines, plural drain lines, plural **thin film transistors** and plural **pixel** electrodes corresponding to the plural **thin film transistors**, and a **drive circuit** area disposed at a periphery of the substrate and having a **drive circuit** for driving the plural **thin film transistors**. The **thin film transistor** has a polycryst. Si **semiconductor** layer formed on the substrate, a gate electrode formed on the polycryst. Si **semiconductor** layer with a gate insulating film interposed therebetween, an insulating film to cover the polycryst. Si **semiconductor** layer, the gate insulating film and the gate electrode, a drain electrode formed on the insulating film and elec. connected to the polycryst. Si **semiconductor** layer, and a source electrode formed on the insulating film, spaced from the drain electrode and elec. connected to the polycryst. Si **semiconductor** layer. The unevenness of a surface of the polycryst. Si **semiconductor** layer is within 10 % of a thickness of the polycryst. Si **semiconductor** layer

L54 ANSWER 6 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:181395 HCAPLUS
TI Liquid crystal display and its production method. [Machine Translation].
IN Abe, Fumiaki; Sato, Takuo
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001066638	A2	20010316	JP 1999-243990	19990830

AB [Machine Translation of Descriptors]. In the liquid crystal display, while guaranteeing retention volume area, the decrease Takamitsu transmissivity and high fine conversion are actualized by being able to point the shading territory between the **pixels**. On insulated transparent substrate 1, the **pixel** electrode 2 for retention volume which forms the retention volume component, dielectric film 3 for retention volume and retention volume wiring 4 is consecutively provided. Insulator film 5 between the layer is provided to cover the retention volume component. On insulator film 5 between the layer, the thin film **semiconductor** layer 7 which possesses the source / drain territory and gate dielectric film provides with the gate electrode which consists of 8 and gate wiring G, forms the **thin film transistor** (**TFT**) for **pixel electrode drive**. To the source territory of thin film **semiconductor** layer 7 signal wiring 15, pull out to the drain territory and connect electrode 16. With drawer electrode 16, connect with the drain territory of thin film **semiconductor** layer, 7 and the **pixel** electrode 2 for retention volume furthermore in upper layer shading membrane connect 19 and **pixel** electrode 22.

L54 ANSWER 7 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:880871 HCAPLUS
TI Active matrix type **semiconductor** display. [Machine Translation].
IN Tanaka, Sachio; Nagao, Akira
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 31 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000347598	A2	20001215	JP 1999-327547	19991117
PRAI JP 1998-326470	A	19981117		
JP 1999-86202	A	19990329		

AB [Machine Translation of Descriptors]. Offer low spending electric power and the active matrix type **semiconductor** display which actualizes high reliability. The active matrix type **semiconductor** display of this invention resolves the counter electrode into 2, gives the electric potential which differs to the counter electrode the 2 respectively, does reversal drive mutually. Like this, because it is possible, to make the voltage of the picture signal low, by doing, to decrease the voltage which is necessary to to operate, is possible **drive circuit**. As the result, it is possible to actualize the decrease of reliable improvement and spending electric power of the component of the **TFT** and the like which forms **drive circuit** and active **matrix circuit**. In addition, because it is possible, to decrease the voltage of the timing pulse which is supplied by **drive circuit** it is possible, to abbreviate boosting circuit, it is possible to actualize the facet product conversion of **drive circuit**.

L54 ANSWER 8 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:317562 HCAPLUS
TI Display. [Machine Translation].
IN Ino, Masumitsu; Nakashima, Yoshiharu; Kaise, Kikuo
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000137245	A2	20000516	JP 1998-311537	19981102

AB [Machine Translation of Descriptors]. Devising the arrangement of the catalyst injection window, expands the effective picture range of the active matrix type display. The display is assembled making use of the transparent substrate above and the base material 101 underneath. The baseplate of these pairs the bonding has been done the specified gap mutually alongside the seal territory 115 of the difference and around. The electro-optic medium of the liquid crystal and the like has filled up to the gap of both baseplates. The counter electrode is formed to the transparent substrate above. In insulated substrate 101 underneath, as **pixel** array section 104 is formed to the center, the vertical **drive circuit** 105 which is formed with the **thin film transistor** and horizontal **drive circuit** 106 is formed around. As for this **thin film transistor** the **semiconductor** thin film which is crystallized and through the gate insulator on the all over side, the gate electrode which is repeated consists. Is provided in the position where catalyst injection window 120 is piled up with seal territory 115 in order to crystallize this **semiconductor** thin film.

L54 ANSWER 9 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:166733 HCAPLUS
TI Production method of **thin film transistor** device and **thin film transistor** device. [Machine Translation].
IN Fukuda, Kaichi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000077665	A2	20000314	JP 1998-241474	19980827

AB [Machine Translation of Descriptors]. In island condition the sepn. decreases the influence to threshold value voltage of the **TFT** due to the quality variation of the around end of the **semiconductor** layer which is formed reproducibility of threshold value voltage improves, obtaining the **TFT** which possesses the satisfactory drive performance, assures the application to the **pixel** electrode baseplate of the liq. crystal display of **drive circuit** one type. With on insulated substrate 13 the 1st and 2nd **semiconductor** layer ion doping is done in around end 16 t of tapered condition of 16 which is etched is processed in island condition and 17 and 17 t, degrdn. the elec. current drive ability of around end 16 t and 17 t the to amorphous by converting, influence to threshold value voltage is decreased.

L54 ANSWER 10 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:49859 HCAPLUS
TI **Thin film transistor** circuit and the **semiconductor** display which uses that. [Machine Translation].
IN Yamazaki, Shunpei; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000022462	A2	20000121	JP 1999-48578	19990225
PRAI JP 1998-118092		19980428		

AB [Machine Translation of Descriptors]. There is not a picture nonuniformity, high definition * offer the **thin film transistor** circuit which is used for the **drive circuit** in order to offer the **semiconductor** display which can obtain the satisfactory picture of high resoln. As for this invention, it is something which guarantees sufficiently the big analog buffer of elec. current capacity by forming the analog buffer which is formed by differential amplification circuit and the elec. current mirror circuit which are used for the **drive circuit** of the active **matrix** type **semiconductor** display due to small **TFT** of channel width, connect that circuit to plural ordinary lines.

L54 ANSWER 11 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:49755 HCAPLUS
TI Nonvolatile memory and **semiconductor device**. [Machine Translation].
IN Yamazaki, Shunpei; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 30 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000022004	A2	20000121	JP 1998-161365	19980525
	US 6323515	B1	20011127	US 1998-138691	19980824
	US 2002043682	A1	20020418	US 2001-970719	20011004
PRAI	JP 1997-249818	A	19970829		
	JP 1998-132750	A	19980427		
	JP 1998-161365	A	19980525		
	US 1998-138691	XX	19980824		

AB [Machine Translation of Descriptors]. The **semiconductor device** which has the nonvolatile memory whose miniaturization is possible is offered. The FAMOS type nonvolatile memory, having **pixel TFT** and **drive circuit** with the **TFT**, the formation it makes just on the baseplate. Like this the **semiconductor** display whose miniaturization is possible by doing, is offered.

L54 ANSWER 12 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:641107 HCAPLUS
DN 131:250482
TI Electronic devices comprising **thin-film transistors** for liquid-crystal displays
IN Young, Nigel D.; Ayres, John R. A.; Edwards, Martin J.
PA Koninklijke Philips Electronics N.V., Neth.; Philips Ab
SO PCT Int. Appl., 19 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9950911	A2	19991007	WO 1999-IB252	19990215
	WO 9950911	A3	19991118		
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 985232	A2	20000315	EP 1999-901842	19990215
	R: DE, FR, GB, NL				
	JP 2002500829	T2	20020108	JP 1999-549076	19990215
	US 6046479	A	20000404	US 1999-274389	19990323
PRAI	GB 1998-6609	A	19980328		
	WO 1999-IB252	W	19990215		

AB A large-area electronic device, such as an AMLCD, has switching **TFTs** (Tp) in a **matrix** and **circuit TFTs** (Ts) in a peripheral **drive circuit**. Both the **TFTs** (Tp, Ts) comprise a field-relief region (130) which has a lower doping concn. (N-) than their drain region (113) and which is present between their channel region (111) and the drain region (113). This field-relief region (130), at least over most of its length, overlaps with the gate (121) in the circuit **TFTs** (Ts) so as to reduce series resistance in the field-relief region (130) by cond. modulation with the gate (121). However, the drain region (113) in the switching **TFTs** (Tp) is offset from overlap with their gate (121) by at least most of the length of their field-relief region (130). This field-relief offset permits the switching **TFTs** (Tp) to have a lower leakage current than the circuit **TFTs** (Ts).

L54 ANSWER 13 OF 13 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:26622 HCAPLUS
DN 106:26622
TI **Thin film transistor**
IN Okamoto, Kotaro
PA Hosiden Electronics Co., Ltd., Japan
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 187367	A2	19860716	EP 1985-116460	19851223
	EP 187367	A3	19871202		
	EP 187367	B1	19920513		
	R: AT, BE, CH, DE, FR, GB, IT, LI, LU, NL, SE				
	AT 76222	E	19920515	AT 1985-116460	19851223
PRAI	JP 1984-279986		19841228		
	EP 1985-116460		19851223		

AB A high-speed **thin film transistor**, easily formable over a wide area and at low cost, comprises a substrate with (1) an impurity-doped amorphous **semiconductor** layer provided on the substrate; (2) a source and a drain electrode in ohmic contact with the amorphous **semiconductor** layer; and (c) a gate electrode, in Schottky contact with the amorphous **semiconductor** layer, on the amorphous **semiconductor** layer between the source and drain electrodes. The transistor is used as an active element of a **drive circuit** formed on a transparent substrate for driving switching elements to select picture element **electrodes** of an active **matrix** liq.-crystal display cell.

L60 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:353933 HCAPLUS
DN 136:362623
TI **Semiconductor device** and method of manufacturing the same
IN Suzawa, Hideomi; Tsunoda, Akira
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 26 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002053669	A1	20020509	US 2001-7361	20011105
	JP 2002141513	A2	20020517	JP 2000-338572	20001107
PRAI	JP 2000-338572	A	20001107		

AB There is provided a structure of a **pixel** TFT (n-channel type TFT) in which an off current value is sufficiently low. In **impurity** regions, a **concn.** distribution of an **impurity** element imparting one cond. type is made to have a concn. gradient, the concn. is made low at a side of a channel formation region, and the concn. is made high at the side of an end portion of a **semiconductor** layer. The **semiconductor device** consists of a thin film transistor (TFT) can be a liq. crystal module, an electroluminescent (EL) module of similar electronic devices.

L60 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:241196 HCAPLUS
DN 136:254662
TI **Semiconductor** display **device** and manufacturing method thereof
IN Ohnuma, Hideto
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 33 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002036288	A1	20020328	US 2001-957915	20010921
	JP 2002190479	A2	20020705	JP 2001-288483	20010921
PRAI	JP 2000-289457	A	20000922		

AB A **semiconductor** display **device** which comprises the polycryst. **silicon** thin film transistors (TFTs) is constructed by a **pixel** region and a peripheral circuit and TFT characteristics required for each circuit are different. For example, an LDD (Lightly Doped Drain) structure TFT having a large off-current suppressing effect is suitable for the **pixel** region. Also, a GOLD (Gate-Overlapped LDD) structure TFT having a large hot carrier resistance is suitable for the peripheral circuit. When the performance of the **semiconductor** display **device** is improved, it is suitable that difference TFT structures are used for each circuit. In the case where the GOLD structure TFT having both Lov regions (low **concn**. **impurity** regions which are overlapped with gate electrode) and Loff regions (low **concn**. **impurity** regions which are not overlapped with gate electrode) is formed, ion implantation into the Lov regions is independently performed using a neg. resist pattern formed in a self alignment by a rear surface exposure method as a mask, and thus **impurity concns**. of the Lov regions and the Loff regions can be independently controlled. Therefore, the GOLD structure TFT having both the hot carrier resistance and the off-current suppressing effect can be formed and the simplification of a manufg. process of the **semiconductor** display **device** and the improvement of performance thereof are compatible with each other.

L60 ANSWER 3 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:172451 HCAPLUS
DN 136:207812
TI **Semiconductor device** with TFTs in **pixel** portion and driver circuit on same substrate and fabrication of same
IN Fujimoto, Etsuko; Murakami, Satoshi; Yamazaki, Shunpei; Eguchi, Shingo
PA Japan
SO U.S. Pat. Appl. Publ., 73 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002028544	A1	20020307	US 2001-916329	20010730
	JP 2002175028	A2	20020621	JP 2001-227219	20010727
PRAI	JP 2000-230401	A	20000731		
	JP 2000-301389	A	20000929		
	JP 2000-301390	A	20000929		

AB A **semiconductor device** having a TFT formed in a **pixel** portion and an n-channel TFT and a p-channel TFT that constitute a driver circuit provided in the periphery of the **pixel** portion, all of the TFTs being formed on the same substrate, wherein the n-channel TFT has a second **concn. impurity** region that partially overlaps a gate electrode, and wherein the p-channel TFT and the TFT formed in the **pixel** portion resp. have second **concn** . **impurity** regions that do not overlap gate electrodes. The **semiconductor device** is specifically a liq. crystal display device. The invention also relates to electronic appliances that employ the liq. crystal display device as a display unit.

09/837,877

L60 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:363338 HCAPLUS
TI Solid-state image pickup device. [Machine Translation].
IN Inoue, Ikuko
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000150848	A2	20000530	JP 1998-317833	19981109
	TW 427023	B	20010321	TW 1999-88119356	19991105
	US 6403998	B1	20020611	US 1999-435464	19991108
PRAI	JP 1998-317833	A	19981109		

AB [Machine Translation of Descriptors]. It is possible, retards blooming and the color mixture to prevent the pouring in to the contiguity **pixel** of the signal which occurs in the territory where the baseplate is deep. On the **semiconductor** substrate, arranging the unit cell which includes the photoelectric conversion section and the signal scan **circuit** in **matrix** two dimension condition, 1st to provide p well territory 21 in the surface of this baseplate 20 making use of N type **Si** baseplate 20 in the **MOS** type solid-state image pickup device which has with the signal conductor which reads out the signal from each cell of the image pickup territory and this image pickup territory which become, as the **semiconductor** substrate, discretionary to provide the 2nd p well territory 31 whose p type high **impurity concentration** is higher than said territory 21 in the surface of this 1st p well territory 21, the photoelectric conversion section 1st The formation it does inside p well territory 21, the formation does the signal scan circuit inside 2nd p well territory 31.

L60 ANSWER 5 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:32335 HCAPLUS
DN 132:173095
TI Epitaxial GaAs x-ray detectors for x-ray astrophysics
AU Bavdaz, Markos; Owens, Alan; Peacock, Anthony J.
CS Astrophysics Div., Space Sci. Dep., ESA, ESTEC, Noordwijk, Neth.
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3768(Hard X-Ray, Gamma-Ray, and Neutron Detector Physics), 451-456
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB In recent years, considerable effort was expended in producing **semiconductor** based x-ray detectors for x-ray astrophysics with high spectral and high spatial resoln. In practical terms, this means producing pixelated detectors, comprising >103 **pixels** each <100 .mu.m in size, with spectral resolving powers, E/.DELTA.E > 20 at 10 keV. While progress at soft x-rays wavelengths was spectacular, largely due to the introduction of x-ray sensitive CCD's, progress at higher energies was slow. This is because traditional high resoln. detectors either suffer from poor detection efficiencies >10 keV, as in the case of **Si** based technol., or are very constrained by cryogenic and fabrication problems as in the case of Ge based detectors. Recent developments in the material science of wide-gap **semiconductors**, and in particular GaAs and CdZnTe, showed that it may now be possible to construct efficient hard x-ray detector with near Fano limited energy resoln. The authors report on hard x-ray measurements with 2 prototype deep depletion epitaxial GaAs detectors of active areas 2.22 mm2 and thicknesses 40 and 400 .mu.m at the ESRF and HASYLAB synchrotron research facilities. Charge collection efficiencies must be >98% and that the material used to produce them is of extremely high purity, with **impurity concns** . <1013 cm-3.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L60 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:549540 HCAPLUS
DN 131:206705
TI 512.times.512-Element GeSi/**Si** heterojunction infrared FPA
AU Wada, Hideo; Nagashima, Mitsuhiro; Hayashi, Kenkichi; Nakanishi, Junji; Kimata, Masafumi; Kumada, Norimasa; Ito, Sho
CS Technical Research and Development Institute, Japan Defense Agency, Setagaya-ku Tokyo, Japan
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3698(Infrared Technology and Applications XXV), 584-595
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB We have developed a monolithic 512 .times. 512 element GeSi/**Si** heterojunction IR focal plane array (FPA). The operation mechanism of the GeSi/**Si** heterojunction detector is the same as that of the PtSi/**Si** Schottky-barrier detector. We have fabricated the GeSi/**Si** heterojunction using MBE technol. and confirmed that ideal strained GeSi films were grown on **Si** substrates. We have evaluated the dependencies of spectral responsivity on the Ge compn., **impurity concn.**, and GeSi thickness, and we have optimized them for 8-12 .mu.m IR detection. The 512 .times. 512 element FPA has a **pixel** size of 34 .times. 34 .mu.m2 and a fill factor of 59%. A low noise equiv. temp. difference of 0.08 K (f/2.0) was obtained with a 300 K background and a very small 2.2% responsivity dispersion.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L60 ANSWER 7 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:613890 HCAPLUS
DN 127:227504
TI Solid-state image sensor with element isolation region of high **impurity concentration** and method of manufacturing the same
IN Morimoto, Michihiro
PA NEC Corp., Japan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5668390	A	19970916	US 1996-629531	19960409
	JP 08288496	A2	19961101	JP 1995-95088	19950420
	JP 2848268	B2	19990120		
PRAI	JP 1995-95088		19950420		

AB Solid-state image sensors having a plurality of photodiodes are described which comprise a P-type layer provided on a surface of a **semiconductor** substrate; an N-type layer provided in the P-type layer; a P+-type region which is disposed on a surface of the N-type layer, the P+-type region and the N-type layer together with the P-type layer constituting each of the photodiodes; and a P++-type region which is disposed in a region surrounding the photodiode excepting in a read region for reading out changes in the photodiode and which has a higher **impurity concn**. and a greater depth than the P+-type region. By forming the P++-type region which isolates photodiode regions and vertical CCD regions from one another as a high **impurity concn**. diffusion layer or an electron trap region contg. a large amt. of electron trap centers, it is possible to reduce smear generation in unit **pixels** and to produce sharp images.

L60 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:56574 HCAPLUS
DN 124:101992
TI Solid-state image pickup device and its manufacture
IN Yoshida, Takuji
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07297378	A2	19951110	JP 1994-83371	19940421

AB The device comprises (A) **matrix**-like arranged **pixel** converting incident light to a signal charge, on 1st conductive-type **semiconductor** substrate, (B) buried channel region corresponding to the **pixel** array and reading the signal charge (through a field shift region), (C) transfer electrode formed on the field shift region and channel region through a gate insulating film, (D) optical shield film having an opening (at the **pixel** region) on the transfer electrode, and (E) a region for breakdown margin and a device-sepg. region under the **semiconductor** substrate of a region between the edge of the transfer electrode and the edge of the optical shield film. Manuf. of the device involves the following steps; (1) successively forming a gate insulating film and 2nd conductive-type buried channel region on 1st conductive-type **semiconductor** substrate, (2) forming a transfer electrode on the gate insulating film above the channel region, and forming 1st conductive-type 1st impurity region neighboring the channel region using the transfer electrode and photoresist pattern as a mask, (3) forming 2nd-conductive type 2nd impurity region (as a **pixel**) on the **semiconductor** substrate of a region neighboring the 1st impurity region, and (4) forming a mask exposing a part of the 1st impurity region and the 2nd impurity region, and injecting the 1st conductive-type impurity into the substrate to form a high-**concn**. **impurity** region.

L60 ANSWER 9 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:287318 HCAPLUS
DN 120:287318
TI **Semiconductor devices**
IN Kochi, Tetsunobu; Myawaki, Mamoru
PA Canon Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05235161	A2	19930910	JP 1992-69863	19920219

AB The device has a control electrode over a 1st-cond. 1st **semiconductor** region as sepd. by an insulating layer, 2nd-cond. 2nd **semiconductor** regions below the both ends of the control electrode, and a 2nd-cond. 3rd **semiconductor** region, which has an **impurity concn.** higher than that in the 2nd **semiconductor** regions, in the 1st **semiconductor** region immediate below the control electrode, for control of connection and sepn. of neighboring devices with a **MOS** transistor structure. Cross-talk between **pixels** and noise level due to dark current are lowered.

L60 ANSWER 10 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:459074 HCAPLUS
DN 117:59074
TI Solid-state image pickup using charge modulation device
IN Matsumoto, Kazuya
PA Olympus Optical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03297169	A2	19911227	JP 1990-99263	19900417

AB In the title pickup using a charge modulation device (CMD) having a metal-insulator-**Si**-type light-receiving part as a **pixel**, the **impurity concn.** of the p-type **semiconductor** substrate of the CMD is 5 x 1013-1 x 1017 cm-3 and the **impurity concn.** of the n-type channel **semiconductor** layer is established corresponding to the change of the **impurity concn.** of the p-type **semiconductor** substrate.

L61 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:349943 HCAPLUS
TI The thin film transistor and the liquid crystal display which uses that. [Machine Translation].
IN Sera, Kenji
PA Nec Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002134753	A2	20020510	JP 2000-322497	20001023

AB [Machine Translation of Descriptors]. In the active matrix type liquid crystal display for the light/write valve which uses LDD structure TFT as **pixel** switchtransistor, in the device the occasion where incidence it can point powerful light, with the incident light to the **semiconductor** active layer of TFT and the reflected light from optical system of the lens and the like in the channel territory and the LDD territory of the TFT section as the optical leak electric current which occurs due to optical excitation becomes problem, miniaturization and high brightness conversion of the projector advance, incident brightness to the light/write valve increasing is to be large accelerating problem has become. The channel territory 6 or the carrier which is formed in the LDD territory 5 is made to recombine to the LDD territory 5 of LDD structure TFT, in the high density impurity territory 7 as the LDD territory 5 by forming the high density impurity territory 7 whose high **impurity concentration** is high with the same electric conduction type, with the invasion of light, the carrier does not reach to the drain or the source, it can actualize the decrease of optical leak electric current with respect to substance by the sea urchin doing.

L61 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:475287 HCAPLUS
TI Thin film transistor substrate and liquid crystal display. [Machine Translation].
IN Nagahiro, Tadao; Chou, Kouyu
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000196094	A2	20000714	JP 1998-371423	19981225

AB [Machine Translation of Descriptors]. In regard to the TFT baseplate, alignment error occurring, the TFT baseplate which can prevent the occurrence of **pixel** defect is offered. With the insulated gate electrode and the both sides of the gate electrode which demarcate the channel inside the transparent insulated substrate and the **semiconductor** thin film and the **semiconductor** thin film which were formed on that, the source of the high high **impurity concentration** which the formation is done / the drain territory and the low high **impurity concentration** territory and the gate electrode of the pair which was formed inside the **semiconductor** thin film with the channel and the source / the drain territory being overturned inside the **semiconductor** thin film, through opening which was formed to the insulator film between the layer which was formed on the transparent insulated substrate and the insulator film between the layer the source of pair / one side of the drain territory was connected electrically the on one hand source / the drain electrode and insulation between the layer Is arranged on the membrane, the low high **impurity concentration** territory of pair covers one side at least, the formation it is done with the layer which is identical with the source / drain electrode, possesses with the shading layer which is separated from the source / drain electrode.

L61 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:206501 HCAPLUS
TI Solid-state image pickup device and its production method. [Machine Translation].
IN Kuriyama, Shunkan
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000091550	A2	20000331	JP 1998-255582	19980909

AB [Machine Translation of Descriptors]. To high sensitivity the solid-state image pickup device and its production method of making convert are offered by decreasing the electric charge accumulation capacity of the photodiode. In the territory inside aforementioned **semiconductor** substrate 11 where light absorbent section the **pixel** which includes with the amplifier circuit which connects 12 of the 2nd electric conduction type which was formed inside **semiconductor** substrate 11 of 1st electric conduction type and aforementioned light absorbent section 12 electrically is arranged, plural touches at least to the portion of the aforementioned light absorbent section 12 base, it designated that diffusion territory 13 of the 1st electric conduction type whose high **impurity concentration** is lower than aforementioned **semiconductor** substrate 11 is formed as feature.

L61 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:341477 HCAPLUS
DN 129:74117
TI Manufacture of active-matrix display devices
IN Shibue, Tsukasa; Yoshinochi, Atsushi; Cho, Koyu; Takeuchi, Akira
PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan; Sharp Corp.
SO Jpn. Kokai Tokkyo Koho, 17 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10144929	A2	19980529	JP 1996-315486	19961112
	US 5923961	A	19990713	US 1997-968025	19971112
PRAI	JP 1996-315486		19961112		

AB N-channel TFTs with self-aligned low-**concn.** **impurity** regions and non-self-aligned source/drain regions are formed in **pixel matrix** area and the N-channel driving regions of peripheral circuit area, and P-channel TFTs with self-aligned source/drain regions are formed in the P-channel driving regions of peripheral circuit area.

L61 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:708569 HCAPLUS
DN 123:100120
TI Thin-film transistor, its manufacture, and liquid-crystal display device using it
IN Inoue, Yuko; Kinoshita, Yukio; Hayashi, Hisao
PA Sony Corp., Japan
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 652595	A2	19950510	EP 1994-117355	19941103
	EP 652595	A3	19971001		
	R: DE, FR, GB				
	JP 07131030	A2	19950519	JP 1993-301337	19931105
	CN 1112730	A	19951129	CN 1994-112822	19941105
	CN 1050939	B	20000329		
	US 6153893	A	20001128	US 1996-764308	19961212
	US 2001014493	A1	20010816	US 1999-433179	19991103
PRAI	JP 1993-301337	A	19931105		
	US 1994-334355	B1	19941103		
	US 1996-764308	A3	19961212		

AB An LDD structure of a thin-film transistor for **pixel** switching is realized on a large glass substrate by low-temp. processes. A thin-film **semiconductor device** for display comprises a display part and a peripheral driving part formed on a glass substrate. **Pixel** electrodes and N-channel LDD-TFTs are arranged in a matrix in the display part. P- and N-channel TFTs are formed in the driving part. Each TFT consists of a gate electrode, an insulating film formed on the gate electrode, a polycryst. **semiconductor** layer formed on the insulating layer, and a high-**concn.** **impurity** layer constituting a source and a drain formed on the polycryst. **semiconductor** layer. Further, an N-channel LDD-TFT for switching has an LDD structure in which a low-**concn.** **impurity** layer is interposed between the polycryst. **semiconductor** layer and the high-**concn.** **impurity** layer.

L61 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:662892 HCAPLUS
DN 117:262892
TI Lateral static induction transistor used as **pixel** of solid-state optical imaging device
IN Suzuki, Mutsumi
PA Nikon Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04139767	A2	19920513	JP 1990-260535	19901001
	US 5424562	A	19950613	US 1994-327847	19941024
PRAI	JP 1990-260535		19901001		
	US 1991-770981		19911001		
	US 1993-8099		19930122		
	US 1993-138879		19931018		

AB The title lateral static induction transistor (LSIT) comprises an epitaxial layer (1) with the same cond. type as that of a **semiconductor** substrate between the substrate and the opposite cond.-type epitaxial layer. The epitaxial layer (1) functions as a buffer region to give uniform elec. characteristics, even though the substrate has fluctuation of an **impurity concn**.

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L71 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:353934 HCAPLUS
DN 136:378324
TI Electro-optical device and method of manufacturing the same
IN Nakajima, Setsuo; Ohnuma, Hideto; Makita, Naoki; Matsuo, Takuya
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 28 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002053674	A1	20020509	US 2001-238	20011102
PRAI	JP 2000-336836	A	20001106		

AB Methods for manufg. **semiconductor devices** are described which include forming an amorphous **semiconductor** layer, doping the layer with a catalytic element for promoting crystn., and heating the doped layer (e.g., using a laser) to produce a cryst. **semiconductor** layer. Devices fabricatable by using the methods are also described which comprise an **n-channel thin-film transistor** and a p-channel **thin-film transistor**. In particular, display devices, esp. liq.-crystal displays, employing the **semiconductor devices** in **pixel** control are described.

L71 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:936068 HCAPLUS
DN 136:45808
TI Light emitting device and manufacturing method thereof
IN Yamazaki, Shunpei; Fukunaga, Takeshi; Koyama, Jun; Inukai, Kazutaka
PA Japan
SO U.S. Pat. Appl. Publ., 37 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001055841	A1	20011227	US 2001-832867	20010412
	JP 2002057162	A2	20020222	JP 2001-118527	20010417
PRAI	JP 2000-115699	A	20000417		

AB Light emitting devices are described comprising an **n-channel TFT** which may be a driver circuit and a light emitting element in each of **pixels**, the **n-channel TFT** comprising: an active layer including: a channel forming region; an n-type impurity region adjacent to the channel forming region; an n-type impurity region adjacent to the n-type impurity region; and an n-type impurity region adjacent to the n-type impurity region; a gate **insulating layer** provided over the active layer; and a gate electrode provided over the gate **insulating layer** including: a first gate electrode provided over the gate **insulating layer**; and a second gate electrode provided over the first gate, wherein the first gate electrode overlaps the channel forming region and the n-type impurity region (c) with the gate **insulating layer** therebetween, and wherein the second gate electrode overlaps the channel forming region with the gate **insulating layer** therebetween. Fabrication methods of the light emitting devices also described. Application of the light emitting devices in electronic devices is noted.

L71 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:774115 HCAPLUS
DN 133:343437
TI **Semiconductor device** and manufacturing method thereof
IN Yamazaki, Shunpei
PA Sel Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 40 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1049167	A2	20001102	EP 2000-108989	20000427
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001094115	A2	20010406	JP 2000-130958	20000428
PRAI	JP 1999-124924	A	19990430		
	JP 1999-206961	A	19990722		

AB A **semiconductor device** having high operating performance and reliability, and a manufg. method thereof are provided. An LDD region 207 provided in an **n-channel TFT** 302 forming a driving circuit enhances the tolerance for hot carrier injection. LDD regions 217-220 provided in an **n-channel TFT** (**pixel TFT**) 304 forming a **pixel** portion greatly contribute to the decrease in the OFF current value. Here, the LDD region of the **n-channel TFT** of the driving circuit is formed such that the concn. of the n-type impurity element becomes higher as the distance from an adjoining drain region decreases.

L71 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:705201 HCAPLUS
DN 133:288962
TI A method for manufacturing an electrooptical device
IN Yamazaki, Shunpei; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 46 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1041641	A2	20001004	EP 2000-105608	20000316
	EP 1041641	A3	20010509		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000349298	A2	20001215	JP 2000-75017	20000317
	CN 1276622	A	20001213	CN 2000-118807	20000326
PRAI	JP 1999-84736	A	19990326		

AB Electrooptical devices (e.g., liq. crystal or electroluminescent displays) having a **pixel** section and a driver circuit over a substrate are described which comprise an **n-channel thin-film transistor** (**TFT**) of the driver circuit having .gtoreq.1 lightly doped drain (LDD) region that at least partly overlaps a gate electrode of the **n-channel TFT** with a gate **insulating film** interposed between them; a **pixel TFT** of the **pixel** section having .gtoreq.1 LDD region that does not overlap the gate electrode of the **pixel TFT** with the gate **insulating film** interposed; and a wiring comprising a first wiring having a same material and formed in a same layer as the gate electrode of the **pixel TFT** laminated with a second wiring having a lower resistivity than the first wiring. The wirings may comprise an input-output signal wiring and a gate wiring; resistivity is steeply reduced in comparison with prior art devices.

L71 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:359810 HCAPLUS
DN 131:163864
TI Polycrystalline **thin-film transistors** on plastic substrates
AU Carey, Paul G.; Smith, Patrick M.; Theiss, Steven D.; Wickboldt, Paul; Sigmon, Thomas W.
CS Lawrence Livermore National Lab., Livermore, CA, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3636(Flat Panel Display Technology and Display Metrology), 4-10
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB Flat panel displays made on plastic substrates are envisioned for use in certain com. and military systems because they are more rugged and lightwt. than displays made on glass substrates. High information content can be attained for such displays using an active matrix array of **thin film transistors** (**TFTs**) for the **pixels** and high current **TFTs** for the drivers. The fabrication of high performance polysilicon **TFTs** on flexible plastic substrates is presented along with corresponding elec. characteristics. Plastic substrates pose severe temp. constraints on the fabrication process. To overcome elec. characteristics. Plastic substrates pose sever temp. constraints on the fabrication process. To overcome these constraints, the authors' group at LLNL used low temp. **silicon**, oxide, and aluminum thin film deposition steps and pulsed excimer laser processing to perform the **TFT** channel crystn. and the source/drain doping. Sheet resistance values <1k.OMEGA./DAL were obtained using the authors' laser doping technique for 900 .ANG. thick polysilicon films. The authors' **n-channel** polysilicon **TFT** elec. performance on plastic shows mobilities up to 50 cm2/V-sec and ON current to OFF current ratios of up to 1 X 106 for gate voltages from -1 to +35 V.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L71 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:493492 HCAPLUS
DN 129:196748
TI Composite **semiconductor** circuit **devices**
IN Otani, Hisashi; Koyama, Jun; Okata, Yasushi; Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10200112	A2	19980731	JP 1996-358953	19961230
	US 6124602	A	20000926	US 1997-998969	19971229
PRAI	JP 1996-358953	A	19961230		

AB The device has a no. of **semiconductor devices** on active regions from a cryst. **Si** film, which has a texture laterally grown parallel to the substrate from desired regions (e.g., where a metal crystn. catalyst is applied to), on an insulating surface of the substrate, and (1) distances between the active layer and the desired regions equal or nearly equal to each other (e.g., for **thin-film transistors** of the same characteristics on the active layers), and (2) distances between p-channel transistors and the desired region differing from those between **n-channel** transistors and the desired region for correction of differences of characteristics between the p- and the **n-channel** transistor on a complementary circuit. Direction of movement of carriers is aligned to growth direction of prismatic crystals in the **Si** film for suppression of short channel effect, and the circuit device can be used for active matrix displays.

L71 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:705963 HCAPLUS
DN 127:365038
TI **TFT semiconductor device** and its fabrication
IN Yamazaki, Shunpei; Fukunaga, Kenji
PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan
SO Jpn. Kokai Tokkyo Koho, 18 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09275216	A2	19971021	JP 1997-40140	19970207
	CN 1168538	A	19971224	CN 1997-103164	19970209
	US 5864151	A	19990126	US 1997-795257	19970210
	US 6194762	B1	20010227	US 1998-206637	19981207
	CN 1227416	A	19990901	CN 1999-102192	19990208
	US 2001007368	A1	20010712	US 2001-774427	20010130
PRAI	JP 1996-48272	A	19960209		
	US 1997-795257	A1	19970210		
	US 1998-206637	A1	19981207		

AB In a **semiconductor device** comprising n- and p-channel **TFTs** on a substrate, LDD regions or offset gates with a relatively wider offset width are selectively formed only for the **n-channel TFTs**, the source and drain regions of the p-channel **TFTs** are doped only with a p-type dopant, and the p-channel **TFTs** have regions doped with n- and p-type dopants next to the source and drain regions. Specifically, the **semiconductor** layers of the **TFTs** contains H and a halogen. A method for fabricating the **TFTs** is also described. The n- and p-channel **TFTs** have very similar transistor properties and are useful as a CMOS **circuit** of an active **matrix** display.

L71 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:505735 HCAPLUS
DN 127:115350
TI Electro-optical device
IN Mase, Akira; Hiroki, Masaaki
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S., 16 pp., Cont. of U.S. Ser. No. 13,240, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5642213	A	19970624	US 1994-247924	19940520
	JP 06027484	A2	19940204	JP 1991-76785	19910315
	JP 2873632	B2	19990324		
	JP 11095264	A2	19990409	JP 1998-205020	19910315
	JP 3220092	B2	20011022		
	JP 11218787	A2	19990810	JP 1998-232502	19910315
	JP 3229938	B2	20011119		
	JP 2001183704	A2	20010706	JP 2000-319873	19910315
	JP 2001209332	A2	20010803	JP 2000-350442	19910315
	JP 2002050769	A2	20020215	JP 2001-146927	19910315
	US 6236064	B1	20010522	US 1995-470598	19950606
PRAI	JP 1991-76785	A	19910315		
	US 1992-846860	B3	19920306		
	US 1993-13240	B1	19930203		
	JP 1998-205020	A3	19910315		
	JP 2000-319873	A3	19910315		
	US 1994-247924	A3	19940520		

AB **Semiconductor devices**, esp. liq.-crystal electrooptical devices, capable of compensating for the operation of any malfunctioning **thin-film transistor** (**TFT**) existing within the device if such a malfunction occurs are described in which plural complementary **TFT** configurations are provided per **pixel** electrode. Each complementary **TFT** configuration consists of at least one p-channel **TFT** and at least one **n-channel TFT**. The input and output terminals of the plural complementary **TFT** configurations are connected in series. One of the input and output terminals is connected to the **pixel** electrode, while the other is connected to a first signal line. All the gate electrodes of the p-channel and **n-channel TFTs** included in the plural complementary **TFT** configurations are connected to a second signal line. The gate electrodes are preferably made of an oxidizable material and are provided with an oxide layer of the material on a surface.

L78 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:450136 HCAPLUS
DN 137:25988
TI Light-emitting device and method of fabricating the same
IN Yamagata, Hirokazu
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S. Pat. Appl. Publ., 27 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002070385	A1	20020613	US 2001-11195	20011207
PRAI	JP 2000-378096	A	20001212		

AB A light-emitting device having a structure in which a mask used for forming a film such as an org. compd. layer does not come in contact with the **pixels** in forming the light-emitting elements is described comprising a **TFT** over a substrate; a light-emitting element over the substrate, the light-emitting element comprising a first electrode, an org. compd. layer and a **second** electrode; a **first wiring** elec. connected to the first electrode and provided over the substrate; an **insulating film** provided over the **first wiring**; and a **second wiring** formed over the **first wiring** and over the **insulating film**, the **second wiring** elec. connected to the **TFT**. A method of fabricating the light-emitting device(e.g., active matrix type) is also described entailing, a partitioning wall constituted by a 2nd wiring and a sepn. portion is formed on the interlayer-**insulating film**, and the **pixels** are surrounded by the partitioning wall, preventing the mask from coming into direct contact with the **pixels**, the mask being used for forming the org. compd. layer and the opposing electrode of the light-emitting elements. Use of the light-emitting device in display device, digital camera, notebook computer, image reprodn. device, goggle-type display, video camera, telephone is indicated.

L79 ANSWER 1 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:466638 HCAPLUS
DN 137:39432
TI Method of fabricating an imager array
IN Possin, George Edward; Kwasnick, Robert Forrest
PA USA
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002076844	A1	20020620	US 2000-681070	20001220
	EP 1217653	A1	20020626	EP 2001-310526	20011217
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
PRAI	US 2000-681070	A	20001220		

AB Reduced mask methods of fabricating an imager array having a plurality of **pixels**, each **pixel** comprising a **thin-film transistor** (**TFT**) and an assocd. photosensor (e.g., a photodiode), are described which entail, for each resp. **pixel**, forming a gate electrode and a photosensor bottom electrode on a substrate; forming a photosensor body disposed on at least a portion of the photosensor bottom electrode; depositing a common **dielec. layer** over the gate electrode and over the photosensor body; forming a **TFT** body on the common **dielec. layer** so that the **TFT** body is disposed above and in a spaced relationship with the gate electrode; depositing a source/drain metal conductive layer over the **TFT** body and over exposed portions of the common **dielec. layer**; removing portions of the source/drain metal conductive layer in accordance with a predetd. pattern so as to expose a portion of an upper surface of the **TFT** body, and so as to leave .gtoreq.1 sacrificial region of source/drain metal remaining disposed on the common **dielec. layer** above the photosensor body; etching the exposed portion of the **TFT** body to form a back channel region in the **TFT** body, the back channel region being disposed over the gate electrode; and then removing the .gtoreq.1 sacrificial region. **Pixels** may be formed simultaneously. Charge retention effects are minimized by the process.

L79 ANSWER 2 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:780521 HCAPLUS
DN 135:325088
TI Self-luminous device and electric machine using the same
IN Koyama, Jun; Inukai, Kazutaka
PA Sel Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 56 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1148553	A2	20011024	EP 2001-109522	20010417
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2002006777	A2	20020111	JP 2001-117529	20010416
	CN 1327270	A	20011219	CN 2001-116648	20010417
PRAI	JP 2000-114592	A	20000417		

AB Self-luminous (e.g., electroluminescent) elements are described in which a gate electrode of a current controlling **thin-film transistor** (**TFT**) formed on an insulator overlaps with a sep. **semiconductor film** with a gate **insulating film** sandwiched therebetween. Gray scale displays may be attained by a time division driving method in which the element provided in a **pixel** is controlled to emit light or not to emit light by means of time, thereby avoiding being affected by fluctuation in characteristic in current controlling **TFTs**. Other elec. devices incorporating the elements or displays are also described.

L79 ANSWER 3 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:731297 HCAPLUS
DN 135:295967
TI Light emitting device and a method of manufacturing the same
IN Yamazaki, Shunpei; Hiroki, Masaaki; Fukunaga, Takeshi
PA Japan
SO U.S. Pat. Appl. Publ., 36 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001026125	A1	20011004	US 2001-817674	20010327
	JP 2001345179	A2	20011214	JP 2001-86520	20010326
PRAI	JP 2000-85910	A	20000327		

AB Light-emitting devices which comprise .gtoreq.1 **thin-film transistor** on an **insulating** surface; an anode (or cathode) elec. connected to the **thin-film transistor**; a cathode (or anode) provided opposite the anode; and a luminous material provided between the anode and the cathode are described in which the anode (or cathode) is surrounded by a bank, and a portion of the bank contains a metal film. Methods of manufg. light-emitting devices are described which entail forming .gtoreq.1 **thin-film transistor** on an **insulating** surface; forming a **pixel** electrode elec. connected to the **thin-film transistor**; forming a bank so as to surround the **pixel** electrode; and forming an electroluminescent material over the **pixel** electrode while charging a portion of the bank with a neg. or pos. charge. The banks ensure that the **pixels** are well defined.

L79 ANSWER 4 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:632001 HCAPLUS
DN 135:188779
TI Manufacture of a **thin film transistor semiconductor device** for use in liquid crystal displays
IN Yamazaki, Shunpei; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 51 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1128430	A2	20010829	EP 2001-104319	20010222
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 2001030322	A1	20011018	US 2001-773543	20010202
	CN 1314715	A	20010926	CN 2001-117390	20010221
	JP 2001313397	A2	20011109	JP 2001-46401	20010222
PRAI	JP 2000-44973	A	20000222		

AB The present invention improves the aperture ratio of a **pixel** of a reflection-type display device or a reflection type display device without increasing the no. of masks and without using a black mask. A **pixel** electrode is arranged so as to partially overlap a source wiring for shielding the gap between **pixels** from light, and a **thin film transistor** is arranged so as to partially overlap a gate wiring for shielding a channel region of the **thin film transistor** from light, thereby realizing a high **pixel** aperture ratio.

L79 ANSWER 5 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:581421 HCAPLUS
DN 135:160218
TI **Semiconductor device** and manufacturing method thereof
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 40 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1122794	A2	20010808	EP 2001-102321	20010201
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 2001040645	A1	20011115	US 2001-774388	20010130
	JP 2001290439	A2	20011019	JP 2001-23509	20010131
	CN 1312590	A	20010912	CN 2001-116881	20010201
PRAI	JP 2000-24540	A	20000201		

AB Methods of manufg. **semiconductor devices** (e.g., electroluminescent displays) are described which entail forming a sepg. layer on a first substrate; forming an **insulating film** on the sepg. layer; forming light-emitting elements on the **insulating film**; attaching a fixing substrate to the light-emitting elements using a first adhesive layer; removing the sepg. layer by exposing it to a gas contg. halogen fluoride to sep. the first substrate; and attaching a second substrate on which color filters are provided to the **insulating film** using a second adhesive layer. Method of manufg. **semiconductor devices** (e.g. liq. crystal displays) are also described which entail forming a sepg. layer on a first substrate; forming an **insulating film** on the sepg. layer; forming an active **layer**, a gate **insulating film**, and gate electrodes on the **insulating film**; forming a first interlayer **insulating film** over the gate electrodes; forming wiring and **pixel** electrodes on the first interlayer **insulating film**; attaching a fixing substrate provided with an opposing electrode on the first substrate using a sealant; injecting a liq. crystal between the **pixel** electrodes and the opposing electrode; removing the sepg. layer by exposing the sepg. layer to a gas contg. halogen fluoride to sep. the first substrate; and attaching a second substrate provided with color filters to the **insulating film** using an adhesive layer. **Semiconductor devices** are also described which comprise an adhesive layer on a substrate; an **insulating film** on the adhesive layer; and light emitting elements on the **insulating film** ,wherein emitted from the light emitting elements is emitted through the substrate. Preferably, the substrate is a plastic substrate provided with color filters under the adhesive layer. **Semiconductor devices** comprising a first substrate comprising an org. material and having **thin-film transistors** (**TFTs**) provided thereon; a second substrate; and a liq. crystal material retained between the first and second substrates, wherein color

filters are provided between the first substrate and the **TFTs**, .a black mask together with the color filters.

L79 ANSWER 6 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:566690 HCAPLUS
DN 135:129669
TI Two-dimensional image detector and fabrication method of the same
IN Izumi, Yoshihiro; Teranuma, Osamu
PA Japan
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001010361	A1	20010802	US 2001-766590	20010123
	JP 2001210855	A2	20010803	JP 2000-19332	20000127
PRAI	JP 2000-19332	A	20000127		

AB The invention relates to a 2-dimensional image detector for detecting a 2-dimensional image formed with light such as X-rays, visible light or IR, and a method of fabricating it. The detector allows charges generated by each photoconductor particle to be smoothly transmitted through a photoconductive layer and thereby ensures effective transmission of charges generated in the photoconductive layer to an active matrix substrate. A 2-dimensional image detector of the present invention includes at least an active matrix substrate having a plurality of **pixel** electrodes , and a photoconductive layer laminated on the **pixel** electrodes. The photoconductive layer **bis** composed of a particulate photoconductor, and a binder contg. a resin that renders volumetric shrinkage upon reaction. The foregoing binder contains either (a) a resin that undergoes volumetric shrinkage when it reacts per se (polymn., crosslinking, or decompn.), (b) a polymerizable monomer to form a resin, or (c) a solvent along with the foregoing resin or polymerizable monomer.

L79 ANSWER 7 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:336571 HCAPLUS
DN 134:334359
TI Active matrix substrate with passivation layer and its manufacture
IN Ibita, Satoshi; Yamaguchi, Hirotaka; Tanaka, Hiroaki; Hayase, Takasuke; Kano, Hiroshi; Kaneko, Wakahiko; Miyahara, Tae; Sakamoto, Michiaki; Nakata, Shinichi
PA NEC Corp., Japan; NEC Kagoshima, Ltd.
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001125134	A2	20010511	JP 1999-304682	19991026

AB The active matrix substrate is manufd. by the steps of (1) forming a transparent electrode and a metal **layer** on a transparent **insulating** substrate, and forming gate electrodes, gate lines, and **pixel** electrodes using 1st mask, (2) forming a gate **insulating layer** and an amorphous **Si** **semiconductor** layer on the gate electrode and processing the gate **insulating layer** and amorphous **Si** layer to desired shape using 2nd mask, (3) forming a passivation layer covering the surface and the side of the amorphous **Si** layer and forming an opening through the passivation layer for contacting the source/drain electrodes with the **Si** layer on the **Si** layer using 3rd mask and forming another opening through the passivation layer and metal layer for exposing the metal oxide layer on the **pixel** electrode, and (4) forming an electrode layer on the passivation layer and the upperside of the opening and forming lines connecting the exposed **Si** layer and the **pixel** electrode and drain lines using 4th mask. The obtained active matrix substrate is also claimed. Channel protective type active matrix substrate in which amorphous **Si** layer is covered with the passivation layer is obtained easily.

L79 ANSWER 8 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:861122 HCAPLUS
DN 134:35121
TI Method for manufacturing an electro-optical device
IN Yamazaki, Shunpei; Koyama, Jun; Yamamoto, Kunitaka; Konuma, Toshimitsu
PA Sel Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 49 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1058314	A2	20001206	EP 2000-112013	20000602
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	TW 447145	B	20010721	TW 2000-89110728	20000601
	JP 2001052864	A2	20010223	JP 2000-166763	20000602
	CN 1284694	A	20010221	CN 2000-122263	20000603
PRAI	JP 1999-158813	A	19990604		

AB Methods for manufg. electrooptical devices entailing forming a plurality of **thin-film transistors** (**TFTs**) over a substrate; forming a plurality of **pixel** electrodes each being connected to each of the plurality of **TFTs**; and forming .gtoreq.1 electroluminescent (EL) layer over the plurality of **pixel** electrodes are described in which the EL layer(s) is(are) selectively formed using an ink jet method. An **insulating film** may be formed over the **TFTs**, the film preferably including at least an upper layer which is resistant to penetration by alkali metals (e.g., from the EL layer).

L79 ANSWER 9 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:258774 HCAPLUS
DN 132:286145
TI Electrooptical devices and manufacture
IN Nakamura, Nobuhiro; Yabushita, Koji; Ito, Isamu
PA Advanced Display K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000111937	A2	20000421	JP 1998-285206	19981007

AB The manufg. process, suitable for forming **thin film transistor** array, comprises the steps of: on a glass substrate, forming a metal film (**Mo**, AlZr, AlNd) from which forming a gate electrode and an auxiliary capacitor/circuit by plasma CVD; forming an **insulating layer** (SiOx, SiNx, SiOxNy), a **semiconductor** functional film layer (a-**Si**, poly-**Si**) and an ohmic contact layer (n+ a-**Si**, n+ poly-**Si**); forming a transparent **pixel** electrode layer (ITO); and forming a **Cr** film layer from which forming a source circuit, a drain electrode and a gate circuit.

L79 ANSWER 10 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:610614 HCAPLUS
DN 131:221344
TI Manufacture of array substrates for display devices
IN Kashimoto, Miyuki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11258634	A2	19990924	JP 1998-63254	19980313

AB Manuf. of an array substrate comprising a substrate, a scanning line, a 1st and a 2nd **insulator layers**, a **semiconductor layer**, a **thin-film transistor** comprising source and drain electrodes connected to the **semiconductor** layer, a signal line **lead** from the drain electrode and crossing the scanning line in near right angle, and **pixel** electrodes elec. connected to the source electrode is claimed. In the above manufg. process, formation of contact holes in multilayers comprising .gtoreq.1 **Si nitride** and **Si oxide** layers are carried out by a single process in an etchant contg. **HF** or its salt. Etching of **Si nitride** and **Si oxide** are carried out simultaneously by a single-step etching.

L79 ANSWER 11 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:12355 HCAPLUS
DN 130:73984
TI Liquid-crystal display device with two gate electrodes each having nonanodizing and anodizing metallic layers and method of fabricating same
IN Hwang, Kwang Jo
PA LG Electronics, Inc., S. Korea
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5852481	A	19981222	US 1997-927088	19970910
PRAI KR 1996-39167		19960910		

AB The method of fabricating a liq.-crystal display device comprises forming first and second gate electrodes on first and second regions, resp., of a substrate. The first and second gate electrodes each include a nonanodizing metallic layer and at least one anodizing metallic layer. The two metallic layers also have different etching selection ratios. A first **insulating layer** is formed on the anodizing metallic layer of the first and second gate electrodes and at least a second **insulating layer** is formed over the substrate. A **thin-film transistor** structure, which utilizes the first gate electrode as a gate, is formed on the second **insulating layer**. The **thin-film transistor** structure includes a **semiconductor layer** on the second **insulating layer** over the first gate electrode, an impurity **semiconductor** layer on first and second portions of the **semiconductor** layer, and first and second source/drain electrodes on the impurity **semiconductor** layer covering the first and second portions of the **semiconductor** layer, resp. The method further includes the steps of depositing a passivation layer over the substrate and forming first and second contact holes. The first contact hole exposes the first source/drain electrode and the second contact hole exposes the second gate electrode. A **pixel** electrode is formed on the passivation layer and in contact with the first source/drain electrode and the second gate electrode.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L79 ANSWER 12 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:353954 HCAPLUS
DN 127:27214
TI Coplanar **thin-film transistors** and manufacture thereof
IN Nakada, Yukihiko; Ayukawa, Michihide; Murata, Yasuaki; Ogata, Hidetake
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09107104	A2	19970422	JP 1995-264182	19951012

AB The transistor has a **semiconductor** layer formed to islands on an insulating substrate and .gtoreq.1 gate **insulating film** having the shape same with or larger than the gate electrode and same with or smaller than the **semiconductor** layer. The **semiconductor** layer may be amorphous or microcryst. SiGe0-1, SiC0-1, Si3N0-4, or SiO0-2. The **semiconductor** layer may be amorphous or microcryst. SiGe0-1, SiC0-1, Si3N0-4, or SiO0-2. The **semiconductor** layer and a 1st gate **insulating film** are formed continuously without breaking of vacuum and patterned.

L79 ANSWER 13 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:353953 HCAPLUS
DN 127:27213
TI Coplanar **thin-film transistors** and manufacture thereof
IN Nakada, Yukihiko; Yoshinochi, Atsushi; Murata, Yasuaki
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09107105	A2	19970422	JP 1995-264183	19951012

AB The transistor has a **semiconductor** layer formed to isolands on insulating substrate, .gtoreq.1 gate **insulating films**, the gate electrode, and the source-drain electrodes connected through contact holes, and a silicide layer on the source-drain region. The **semiconductor** layer may be SiGe0-1, SiC0-1, Si3N0-4, SiO0-2, and no silicide layer is formed on the gate electrode.

L79 ANSWER 14 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:624834 HCAPLUS
DN 125:261515
TI **Semiconductor device, thin film transistor**, their manufacture, and display device
IN Abe, Hisashi; Taguchi, Eiji; Oda, Nobuhiko; Segawa, Yasuo
PA Sanyo Denki Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 12
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08195494	A2	19960730	JP 1995-124028	19950523
PRAI JP 1994-112874		19940526		
JP 1994-285190		19941118		

AB The **semiconductor device** includes an **insulating film** of bilayer structure contg. an oxide **film** and an **insulating film**. The transistor includes a gate-**insulating film** of above structure. The oxide film may be oxidized **Si**, preferably by UV-O3 irradn. or by RTA process with lamp light irradn. (by scanning). The **insulating film** may be formed on the oxide film by deposition. The manuf. for the transistor comprises these steps; forming **Si film** on am **insulating** substrate, forming the bilayer gate-**insulating film** on the **Si** film, forming a gate wiring on the gate-**insulating film**, and forming a source/drain region in the **Si** film by self-alignment process. The display device includes the transistor as a **pixel**-driving device. The device shows low interface-level concn., providing the display device with excellent image quality.

L79 ANSWER 15 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:409673 HCAPLUS
DN 125:73843
TI **Semiconductor devices, thin-film transistors**, their manufacture, and imaging devices
IN Nakanishi, Shiro
PA Sanyo Denki Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08088374	A2	19960402	JP 1995-125317	19950524
PRAI JP 1994-118844		19940531		
JP 1994-168407		19940720		

AB The **semiconductor devices** contain a re-oxidized layer between an interface of a **Si** layer and a **Si** oxide layer. The **Si** layer may be formed on an insulator substrate. The manufg. process includes (forming a **Si layer** on an **insulator** substrate,) forming a **Si** oxide layer on the **Si** layer, and forming the re-oxidized layer on the interface of the **Si** layer and the **Si** oxide film. The re-oxidn. layer may be formed by thermal treatment in moisture, high-pressure moisture, or O plasma. Thermal treatment in N after formation of the re-oxidized layer may be involved. The title **thin-film transistor** (**TFT**) contains a re-oxidized layer in an interface of **Si** layer as an active layer and a gate oxidized film which are formed by the above manufg. process. Manuf. of **TFT** contains formation of a **Si layer** on the **insulator** substrate, a **Si** oxide film, and a re-oxidized film successively as above process, formation of a gate electrode on the **Si** oxide film, and formation of a source area and a drain area on the **Si** layer by self-adjustment. Manuf. of a **TFT** contg. forming an interlayer **insulation film** on all over the device, forming a contact hole on the interlayer **insulator film** which contacts with the source area and the drain area, and forming a source electrode and a drain electrode is also claimed. An imaging device with the **TFT** as a **pixel** driving device is also claimed. Required time for the thermal treatment on the manuf. of the gate oxidn. film is shortened.

L79 ANSWER 16 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:761865 HCAPLUS
DN 123:273565
TI Radiation imager with common passivation dielectric for gate electrode and photosensor
IN Wei, Ching Yeu; Salisbury, Roger S.; Kwasnick, Robert F.; Giambattista, Brian W.
PA General Electric Co., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5435608	A	19950725	US 1994-261592	19940617
	US 5480810	A	19960102	US 1995-384093	19950206
PRAI	US 1994-261592		19940617		

AB A solid state radiation imager **pixel** having a **thin film transistor** (**TFT**) coupled to a photodiode in which the photodiode and the **TFT** each comprise a common **dielec. layer**, i.e., a single **dielec. layer** that extends across the **pixel** and that has a gate **dielec. layer** portion and a photodiode body passivation portion. The common **dielec. layer** comprises a monolithic **dielec.** material such as **silicon nitride** or **silicon oxide**. Further, the bottom electrode of the photosensor body and the gate electrode are each disposed on a common surface of the substrate and comprise the same conductive material, the conductive material having been deposited on the **pixel** in the same deposition process. The source and drain electrodes and the common contact electrode for the photodiode each comprises the same source/drain metal conductive material, the conductive material having been deposited on the **pixel** in the same deposition process.

L79 ANSWER 17 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:245401 HCAPLUS
DN 116:245401
TI **Thin-film transistor** for flat panel display and its manufacture
IN Chan, Q.
PA Samsung Electron Devices Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 03190141	A2	19910820	JP 1989-322458	19891212

AB A **thin-film transistor** for a flat panel display having a double-layered gate electrode and a triple-**layered** gate **insulating layer** between the gate electrode and the **semiconductor** lager is manufd. by formation of a 1st gate electrode and a storage capacitor followed by coating the 1st gate electrode with a .apprx.300 .ANG. **Ta** film to form a 2nd gate electrode, formation of a 1st gate **insulating layer** consisting of a Ti2O5 film on the 2nd gate electrode by anodic oxidn. followed by vapor deposition of a 1000-3000 .ANG. SiO2 film using a plasma chem. vapor app. to form a 2nd **insulating layer**, formation of a **pixel** electrode on the 2nd **insulating layer** and setting up the **pixel** electrode ready to contact with a drain electrode in a later step, coating the **pixel** electrode and the 2nd gate **insulating layer** with a .apprx.3000 .ANG. SiO2 film to form a 3rd **insulating layer**, and formation of a **semiconductor** layer, an Ohm layer, a source electrode, and a drain electrode on the 3rd **insulating layer**. The process prevents leak current of the **thin film transistor**.

L79 ANSWER 18 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:548243 HCAPLUS
DN 115:148243
TI Manufacture of array of **thin-film transistors**
IN Kawase, Ryuichi; Hoshino, Akihiro; Toki, Sotaro; Yamamura, Yasushi; Nagase, Toshiro
PA Toppan Printing Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03049237	A2	19910304	JP 1989-184381	19890717
	JP 2778133	B2	19980723		

AB The process includes: (a) forming a transparent elec. conductive film on a glass substrate; (b) printing a resist film with a pattern for drains, **pixel** electrodes, source electrodes, and source-electrode interconnections; (c) patterning the elec. conductive film by etching with the resist as a mask; (d) forming a Ni, Cu, or Au film on the source electrodes and the interconnections; (e) forming a **semiconductor** layer, (e.g., **Si**), an **insulator film** (e.g., **Si** nitride), and an Al or **W-Si** elec. conductive film; (f) printing a resist film with a pattern for gate electrodes and gate-electrode interconnections on the elec. conductive film; (g) forming the gate electrodes and the gate-electrode interconnections by etching the elec. conductive film with the resist film as a mask; and (h) patterning the **insulator layer** and the **semiconductor** layer by etching with the gate electrodes and gate-electrode interconnections as a mask. The source electrodes and source-electrode interconnections have decreased resistance.

29jul02 13:58:18 User267149 Session D244.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2002/Jul W4
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File 6:NTIS 1964-2002/Aug W2
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File 8:Ei Compendex(R) 1970-2002/Jul W2
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File 34:SciSearch(R) Cited Ref Sci 1990-2002/Jul W4
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*File 34: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
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(c)2002 Japan Science and Tech Corp(JST)
*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Jun
(c) 2002 The HW Wilson Co.
File 108:Aerospace Database 1962-2002/Jul
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File 238:Abs. in New Tech & Eng. 1981-2002/Jul
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File 305:Analytical Abstracts 1980-2002/Jul W2
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Jan
(c) 2002 DECHEMA
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200247
(c) 2002 Thomson Derwent
*File 350: Alerts can now have images sent vial all delivery methods. See HELP ALERT and HELP PRINT for more info.
File 344:Chinese Patents Abs JuL 1985-2002/JuL
(c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Mar(Updated 020702)
(c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.

07/29/2002 09/837,877

Alerts have been run. See HELP NEWS 347 for details.
File 371:French Patents 1961-2002/BOPI 200209

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Set     Items   Description
S1     592574   (SEMICONDUCT??????(N1)DEVICE? ?)
S2    2420959   SEMICONDUCT?????
S3       7253   CC=B2560                  Semiconductor devices
S4       4907   MC=S01-G02B
S5    2423801   S1:S4
S6     179020   PIXEL? ?
S7       4960   PIXEL? ?(4N)(MATRIX?? OR MATRIC??)
S8      25713   (MATRIX?? OR MATRIC??)(3N)(CIRCUIT? ? OR LOOP? ? OR PATH? ?
              OR ROUTE? ? OR ELECTRODE? ?)
S9      29849   S7:S8
S10    174342   DRIV?(3N)(CIRCUIT? ? OR LOOP? ? OR PATH? ? OR ROUTE? ? OR -
              ELECTRODE? ?)
S11     47746   TFT OR (THIN()FILM()TRANSISTOR? ?)
S12     24456   TFT OR (THIN()FILM()TRANSISTOR? ?)(3N)PIXEL? ?
S13     47746   S11:S12
S14     31918   N()CHANNEL? ?
S15     25207   (WIRING OR WIRE? ?)(3N)LINE? ?
S16     80206   (FIRST OR ONE OR SECOND OR TWO)(3N)(WIRING OR WIRE? ?)
S17    100165   S15:S16
S18    437979   (INSULAT?????? OR DIELECTRIC???)(3N)(LAYER??? OR FILM??? OR
              COAT??? OR MULTILAYER??? OR SPACER??)
S19     28722   (FIRST OR ONE OR SECOND OR TWO)()(INSULAT?????? OR DIELECT-
              RIC???)
S20     12575   MC=(U11-C06A1B OR U11-C07C3 OR U11-C08A1 OR U11-C08A6)
S21     27735   CC=(A5150 OR A7700 OR B2800 OR B2810 OR B2830)
S22    479119   S18:S21
S23    133409   ONO OR OXIDE(N2)SILICON OR OXIDE(N2)NITRIDE OR SILICON(N3)-
              OXIDE
S24     40865   IMPURIT???(3N)CONCENTRAT????
S25     56287   STORAGE(3N)(CAPACIT??????? OR CONDENS????)
S26    234592   (LOW OR LOWER)(3N)(POWER OR VOLT OR V OR POTENTIAL)
S27      1139   (LOW OR LOWER)(3N)(ELECTRIC??(3N)POTENTIAL)
S28    234676   S26:S27
S29   4356443   TANTALUM OR TA OR CHROMIUM OR CR OR TITANIUM OR TI OR TUNG-
              STEN OR W OR MOLYBDENUM OR MO OR SILICON OR SI
S30      9142   S29 AND S17
S31   3963845   TANTALUM OR TA OR TITANIUM OR TI OR BARIUM OR BA OR HAFNIUM
              OR HF OR BISMUTH OR BI OR TUNGSTEN OR W OR THORIUM OR TH OR -
              LEAD OR PB
S32     67852   S31 AND S22
S33      2274   S5 AND S9
S34         7   S33 AND S30
S35         7   RD (unique items)
S36      2267   S33 NOT S35
S37        35   S36 AND S32
S38        17   S37 AND S13
S39         1   S38 AND S14
S40        16   S38 NOT S39
S41         3   S40 AND S23
S42         3   RD (unique items)
S43        13   S40 NOT S42
S44         1   S43 AND S24
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S45	12	S43 NOT S44
S46	0	S45 AND S25
S47	1	S45 AND S28
S48	11	S45 NOT S47
S49	2239	S33 NOT S37
S50	2	S49 AND S32
S51	370	S33 AND S10
S52	165	S51 AND S13
S53	13	S52 AND S14
S54	13	RD (unique items)
S55	152	S52 NOT S53
S56	4	S55 AND S17
S57	4	RD (unique items)
S58	148	S55 NOT S57
S59	49	S58 AND S22
S60	7	S59 AND S23
S61	7	RD (unique items)
S62	42	S59 NOT S61
S63	2	S62 AND S24
S64	40	S62 NOT S63
S65	1	S64 AND S28
S66	39	S64 NOT S65
S67	1	S66 AND S25

35/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014470652
WPI Acc No: 2002-291355/200233
XRAM Acc No: C02-085438
XRPX Acc No: N02-227490
Active matrix liquid crystal display device has display area having set of pixel regions with respective first thin film transistors, and driving-circuit-forming area having second thin film transistors
Patent Assignee: HITACHI MFR CO LTD (HITA); HITACHI LTD (HITA)
Inventor: HASEGAWA A
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020021380	A1	20020221	US 2001919916	A	20010802	200233	B
JP 2002131783	A	20020509	JP 2001218144	A	20010718	200234	
CN 1337590	A	20020227	CN 2001125207	A	20010809	200234	

Priority Applications (No Type Date): JP 2000241472 A 20000809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020021380	A1		12	G02F-001/1343	
JP 2002131783	A		9	G02F-001/1368	
CN 1337590	A			G02F-001/136	

Abstract (Basic): US 20020021380 A1
Abstract (Basic):
NOVELTY - An active matrix liquid crystal display device has display area having a set of pixel regions with respective first thin-film transistors (TFT). A driving-circuit-forming area having second TFTs is located outside the display area. A gate electrode of first TFT is made of a material different than gate signal line. A gate electrode of second TFT is made of a material different than wiring layer.

DETAILED DESCRIPTION - An active matrix liquid crystal display device consists of a display area and a driving-circuit-forming area outside the display area.

The display area includes a set of pixel regions, each having a first thin-film transistor (TFT).

The driving-circuit-forming area has second TFTs.

The gate electrode of first TFT is made of a material that is different than a gate signal line (GL). The gate electrode of first TFT is electrically connected to the gate signal line.

The gate electrode of each second TFT is made of a material that is different than a wiring layer or electrode. The gate electrode of second TFT is electrically connected to the wiring layer or electrode.

The gate electrodes (GT) of first and second TFTs are made of the same material.

The gate signal **line** and the **wiring** layer or electrode are made of the same material.

USE - As active matrix liquid crystal display device.

ADVANTAGE - Integration densities of gate-signal-line driving circuit and drain-signal-line driving circuit are increased.

DESCRIPTION OF DRAWING(S) - The figure is a plan view showing the structure of each **pixel** of the inventive active **matrix** display device.

Semiconductor layer (AS)
Drain signal line (DL)
Gate signal line (GL)
Gate electrodes (GT)
Pixel electrode (PIX)
pp; 12 DwgNo 1A/7

35/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012289787
WPI Acc No: 1999-095893/199908
XRPX Acc No: N99-069665
Two-terminal active **wire electrode** structure for active **matrix** liquid crystal display - has wire placed in grooves in transparent substrate and covered by insulating layer and-or **semiconductor** layer
Patent Assignee: GL DISPLAYS INC (GLDI-N)
Inventor: GE S; GE Y
Number of Countries: 082 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9900695	A1	19990107	WO 98US11152	A	19980603	199908	B
US 5892558	A	19990406	US 97883117	A	19970626	199921	
AU 9878057	A	19990119	AU 9878057	A	19980603	199922	
EP 991975	A1	20000412	EP 98926157	A	19980603	200023	
			WO 98US11152	A	19980603		
JP 2002513513	W	20020508	WO 98US11152	A	19980603	200234	
			JP 99505540	A	19980603		

Priority Applications (No Type Date): US 97883117 A 19970626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9900695	A1	E	35	G02F-001/133	
	Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW				
US 5892558	A			G02F-001/136	
AU 9878057	A				Based on patent WO 9900695
EP 991975	A1	E		G02F-001/133	Based on patent WO 9900695
	Designated States (Regional): DE FR GB IT				
JP 2002513513	W		39	H01L-049/02	Based on patent WO 9900695

Abstract (Basic): WO 9900695 A
The electrode structure comprises at least **one** conductive **wire** (30) having a **semiconductor** and-or insulating layer (32) over it. The wire and/or layer are attached to a transparent substrate (34). The wire is preferably attached to the substrate by means of an ultraviolet cured adhesive. The substrate defines grooves (38) into which the wire is placed. An array of separated electrodes (40) is formed on the substrate. The conductive wire, the layer(s) and the electrodes form an array of diodes connected in parallel. A first voltage is applied across the conductive wire and the electrodes to turn on the diodes, and a second voltage is applied across the wire and the electrodes to turn off the diodes. Preferably, the substrate comprises glass or plastic. Preferably, the wire includes

tantalum or **chromium**, and the insulating layer and/or **semiconductor** layer comprises **tantalum** oxide, or **silicon** nitride or organic layer. Preferably, the electrodes comprise transparent indium-tin-oxide, **tantalum** or **chromium**
.

ADVANTAGE - Enables large screen display to be made at reasonable cost.

35/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010584124
WPI Acc No: 1996-081077/199609
Related WPI Acc No: 2002-036228
XRAM Acc No: C96-026592
XRPX Acc No: N96-067466

Semiconductor IC for drive **circuit** e.g. active **matrix circuit**, LCD - has triangle shaped sidewalls on both sides of gate electrode and gate wiring

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7321337	A	19951208	JP 94137987	A	19940526	199609	B

Priority Applications (No Type Date): JP 94137987 A 19940526
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7321337	A		16	H01L-029/786	

Abstract (Basic): JP 7321337 A

The **semiconductor** IC has an N-channel type thin film transistor. The anodic film is formed by performing the anodic oxidation of material which constitutes the gate electrode and gate wiring. An insulation film (110) is formed adjoining a **silicon** nitride film (108), which covers the entire active region. The insulation film is etched to leave triangular shaped sidewalls adjoining gate structure.

USE/ADVANTAGE - In image sensor, microprocessor, **semiconductor** memory. Prevents breakage of **second** layer **wiring**.

35/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009357021
WPI Acc No: 1993-050500/199306
XRPX Acc No: N93-203212
Semiconductor memory circuit esp. for DRAM - has level difference between wiring layers formed over gate electrodes of memory cell array selection transistor MISFET and peripheral circuit MISFET and formed in same conductor layer limited to less than 1.5~um
Patent Assignee: HITACHI DEVICE ENG CO LTD (HISD); HITACHI KEISOKU KK (HITA-N); HITACHI LTD (HITA)
Inventor: ASAYAMA K; ENDO K; KANEKO Y; MIYAZAWA H; NAGAO M; OGISHIMA A; SOEDA H; SUWANAI N; UCHIYAMA H; WATANABE K; YONEOKA T
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 5003301	A	19930108	JP 91310425	A	19911126	199306	B
US 5237187	A	19930817	US 91799541	A	19911127	199334	
US 5389558	A	19950214	US 91799541	A	19911127	199512	
			US 93104014	A	19930810		
US 5631182	A	19970520	US 91799541	A	19911127	199726	
			US 93104014	A	19930810		
			US 94327861	A	19941018		
US 6043118	A	20000328	US 91799541	A	19911127	200023	
			US 93104014	A	19930810		
			US 94327861	A	19941018		
			US 97800018	A	19970213		
KR 249268	B1	20000315	KR 9121392	A	19911127	200122	

Priority Applications (No Type Date): JP 90329122 A 19901130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 5003301	A		20	H01L-027/108	
US 5237187	A		32	H01L-027/02	
US 5389558	A		32	H01L-021/70	Div ex application US 91799541 Div ex patent US 5237187
US 5631182	A		31	H01L-021/8242	Div ex application US 91799541 Div ex application US 93104014 Div ex patent US 5237187 Div ex patent US 5389558
US 6043118	A			H01L-021/8242	Div ex application US 91799541 Div ex application US 93104014 Cont of application US 94327861 Div ex patent US 5237187 Div ex patent US 5389558 Cont of patent US 5631182
KR 249268	B1			H01L-027/10	

Abstract (Basic): US 5237187 A
The **semiconductor** memory circuit has each memory cell constituted by a series circuit of a memory cell selecting MISFET and

an information storage stacked capacitor. In a memory cell array region, ther is a MISFET with a gate electrode and source and drain regions, two capacitor electrodes and a dielectric film extended over a first insulating film and over the gate electrode, a second insulating film located on the second capacitor electrode and a third insulating film located between the first insulating film and first capacitor electrode; and a **first wiring** positioned on the **second** insulating film.

In a peripheral circuit region, there is a second MISFET with a gate electrode and source and drain regions, a first insulating film on the gate electrode; a second insulating film on a third insulating film, the third insulating film located between the first and second insulating films, and a **second wiring** on the **second** insulating film. The **second wiring** is formed by the same level conductor layer as that forming the **first wiring**. Similarly, the **first** through third insulating films of the first region are correspondingly associated with the first through third insulating films of the second region, respectively.

USE/ADVANTAGE - Also suitable for SRAM. Improved integration density, product yield and reliability.

Dwg.1/20

Abstract (Equivalent): US 5631182 A

A method for fabricating a **semiconductor** memory circuit device having an array of memory cells arranged in a matrix form and each consisting of a first MISFET and an information storing capacitor both connected in series with each other, and also having a peripheral circuitry constituted by a plurality of second MISFETs, said method comprising:

(a) a step of forming a first gate electrode of each said first MISFET and a second gate electrode of each said second MISFET over first and second regions, respectively, of a first electroconductivity type **semiconductor** substrate;

(b) a step of introducing first impurities of a second electroconductivity type, opposite to the first electroconductivity type, into said **semiconductor** substrate in self-alignment with said first and second gate electrodes, so as to form first **semiconductor** regions for the first and second MISFETs;

(c) a step of forming a side wall insulating film along end portions of said first and second gate electrodes;

(d) a step of forming a first electrode of said information storing capacitor so as to be in contact with one of the source and drain regions of said first MISFET;

(e) a step of forming a dielectric film and a second electrode of said information storing capacitor on said first electrode;

(f) a step of forming a second insulating film over said first and second regions of said **semiconductor** substrate, overlying the second gate electrode over the second region and overlying the second electrode over the first region;

(g) a step of forming a **wiring** layer over said **second** insulating film in said first and second regions;

(h) a step of introducing second impurities of said second electroconductivity type into said **semiconductor** substrate over said second region in self-alignment with said second gate electrode and said side wall insulating film, so as to form second

semiconductor regions for said second MISFETs, after having carried out processes (a) and (c); and

(i) a step of forming a third insulating film overlying only said second region,

wherein said process (h) is carried out prior to said processes (i) and (f), and said process (i) is carried out between said processes (c) and (g).

Dwg.1/20

US 5389558 A

The method for fabricating a **semiconductor** memory **circuit** device having a **matrix** array of memory cells, each contg. a first MISFET and an information storing capacitor connected in series, and peripheral circuitry including second MISFETs. The method comprises forming a first gate electrode of each first MISFET and a second gate electrode of each second MISFET in two regions, respectively, on a **semiconductor** substrate. First N-type impurities are introduced into the substrate in self-alignment **w** .r.t. the two gate electrodes to form source and drain regions for the two MISFETs. A third insulating film is formed in both regions on the substrate, and is partially removed to expose one of the source and drain regions of the first MISFET.

A first electrode of the capacitor is formed in contact with the exposed source or drain region of the first MISFET. A dielectric film and a second capacitor electrode are formed in sequence on the first electrode, and a second insulating film is formed on the third insulating film in the two regions of the substrate. A wiring layer is formed on the second insulating film in the two regions, and the two electrodes extend on the third insulating film in the first region. The thickness of the third insulating film is larger than a total thickness of the two capacitor electrodes.

USE/ADVANTAGE - E.g. for microcomputer circuit incorporating DRAM or SRAM. Improved integration density and product yield during mfr.

Dwg.1/20

35/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05810005
MANUFACTURE OF ACTIVE **MATRIX CIRCUIT**

PUB. NO.: 10-093105 [JP 10093105 A]
PUBLISHED: April 10, 1998 (19980410)
INVENTOR(s): ENOMOTO TAKASHI
TAKAMATSU OSAMU
MIZUTOME ATSUSHI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-229102 [JP 97229102]
FILED: August 26, 1997 (19970826)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce generation rate for short circuit by forming a cathode oxidation metal film by means of anodic oxidation of a gate wire followed by providing thereon SiN:H (**silicon** nitride layer containing hydrogen, nitrogen atoms), so as to form interline insulating layers between a gate and a drain, and between a source and a gate.

SOLUTION: An Al gate line 2 is patterned on an insulating substrate 1, and an Al(sub 2)O(sub 3) insulating film 9 is formed on the surface by anodic oxidation. A pixel electrode 3 is formed of a transparent conductive film, a gate-insulating film 7 of SiN:H, a **semiconductor** layer 4 of amorphous **silicon** and an n(sup +) amorphous **silicon** layer 8 are deposited by using a plasma CVD method for being patterned in a prescribed shape, and finally forming a source **line** 5, a drain **wire** 6. Al(sub 2)O(sub 3) is a film without pin holes, while forming a double-layer structure to the gate insulating film 7 of SiN:H, and to the Al(sub 2)O(sub 3) insulating film 9, and when Al(sub 2)O(sub 3) is formed to at least about 200 angstroms , a short-circuit generation rate between gate-drain and between source-gate can be reduced.

35/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05710569
ACTIVE **MATRIX** PANEL AND DRIVING **CIRCUIT** FOR THE SAME

PUB. NO.: 09-325369 [JP 9325369 A]
PUBLISHED: December 16, 1997 (19971216)
INVENTOR(s): MISAWA TOSHIYUKI
OSHIMA HIROYUKI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-025683 [JP 9725683]
FILED: February 07, 1997 (19970207)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain an active matrix panel which is of optically fine and is of compact and is excellent in reliability by alternately arranging plural first wirings and plural second wirings and alternately arranging first **silicon** thin films and second **silicon** thin films in between adjacent **first wiring** and **second wiring**.

SOLUTION: Unit cells of a driver circuit are formed in areas 196-198 surrounded by a broken **line** which includes a **wiring** for positive power source 184, a wiring for negative power source 185, silicone thin films 186-191 of P type TFTs and silicone thin films 192-195 of N type TFTs. Since the separating of elements of respective TFTs is performed by etching silicone thin films in island shapes, for example, the distance (a) between the island 192 of the **silicon** thin film for the N type TFT and the island 187 of the **silicon** thin film for the P type TFT and the distance (b) between two islands 187, 188 of the silicone thin films for the P type TFTs can be made almost equal. Thus, the degree of integration of a direction along which the unit cells is repeated is enhanced by alternately arranging islands of the P type TFTs and islands of the N type TFTs.

35/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04335186
MEMORY DEVICE

PUB. NO.: 05-326886 [JP 5326886 A]
PUBLISHED: December 10, 1993 (19931210)
INVENTOR(s): SUGIUCHI HIROYUKI
APPLICANT(s): NEC KYUSHU LTD [423996] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-124810 [JP 92124810]
FILED: May 18, 1992 (19920518)
JOURNAL: Section: E, Section No. 1521, Vol. 18, No. 144, Pg. 36, March 10, 1994 (19940310)

ABSTRACT

PURPOSE: To enhance a memory device in degree of integration by a method wherein two gate electrode wirings to serve as the gate electrodes of a pair of transistors are made to overlap each other on an element isolating insulating film through the intermediary of an insulating film.

CONSTITUTION: An element isolating insulating film 2 is selectively formed on a P-type **silicon** substrate 12, and active regions 1 demarcated as surrounded by the element isolating insulating film 2 are arranged in **matrix**. A **first** gate **electrode wiring** 34 is formed of a first polysilicon layer constituting a gate electrode 14 of a transistor formed on the right side of the active region 1 and a word line 24 on an interlayer insulating film 8. Then, a **second** gate electrode **wiring** 44 is formed of a second polysilicon layer constituting a gate electrode 14 of a transistor formed on the left side of the active region 1 and a word line 24 on the interlayer insulating film 8, and the gate electrode wirings 34 and 44 are made to overlap each other through the intermediary of an insulating film 5 on the interlayer insulating film 8.

39/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010320536
WPI Acc No: 1995-221808/199529
Related WPI Acc No: 1995-221804; 1998-227031; 2002-245781
XRPX Acc No: N95-173878

Thin film **semiconductor** integrated circuit e.g. MOSFET for display drive circuit or SRAM - has peripheral drive circuits formed along with active **matrix circuit** made from **thin film transistors** in same package

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME); TAKEMURA Y (TAKE-I); YAMAGUCHI N (YAMA-I); ZHANG H (ZHAN-I)
Inventor: TAKEMURA Y; YAMAGUCHI N; ZHANG H
Number of Countries: 004 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7135324	A	19950523	JP 93301174	A	19931105	199529	B
US 5648277	A	19970715	US 94334335	A	19941102	199734	
CN 1111815	A	19951115	CN 94119925	A	19941105	199737	
US 6218678	B1	20010417	US 94334335	A	19941102	200123	
			US 97815070	A	19970311		
US 20010007357	A1	20010712	US 94334335	A	19941102	200143	
			US 97815070	A	19970311		
			US 2001769374	A	20010126		
US 20010014496	A1	20010816	US 94344335	A	19941122	200149	
			US 97815070	A	19970311		
			US 2001779826	A	20010209		
KR 294088	B	20010917	KR 9428842	A	19941104	200231	

Priority Applications (No Type Date): JP 93301174 A 19931105; JP 93301176 A 19931105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7135324	A		9	H01L-029/786	
US 5648277	A		17	H01L-021/336	
CN 1111815	A			H01L-021/00	
US 6218678	B1			H01L-029/04	Div ex application US 94334335 Div ex patent US 5648277
US 20010007357	A1			H01L-021/425	Div ex application US 94334335 Div ex application US 97815070 Div ex patent US 5648277 Div ex patent US 6218678
US 20010014496	A1			H01L-021/336	Div ex application US 94344335 Div ex application US 97815070 Div ex patent US 5685302 Div ex patent US 6218678
KR 294088	B			H01L-029/78	Previous Publ. patent KR 95015820

Abstract (Basic): JP 7135324 A

The device has its P type (121) and N type (123) low-concentration impurity domains holding their respective impurity domains (120,122) formed on the ground **insulating film** (102) laid above the

substrate (101). A **titanium** metal film (124) laid above them forms the silicide domains (125-127).

The inter-**layer insulating** material (128) is then placed over them and an amorphous silicon (129) is added on one side. The device is equipped with metal wires (133-136) made from nitride **titanium** alloy that connect to the silicide domains and the N type micro-crystal silicon (130,131). The N type impurity domain, P type impurity domain, and the amorphous silicon form the **N channel** peripheral drive circuit (137), the P channel peripheral drive circuit (138), and the active **matrix circuit** (139), respectively.

ADVANTAGE - Provides optimised performance from single package.

Dwg.2/4

Abstract (Equivalent): US 5648277 A

A method of mfg. a **semiconductor device** comprising the steps of:

forming a **semiconductor layer** on an **insulating** surface;

forming a **first insulating film** on the **semiconductor** layer;

forming a gate electrode on the **first insulating film**;

forming a first anodic oxide film on side surfaces of the gate electrode by applying an electric current to the gate electrode in an electrolyte;

etching the **first insulating film** in order to thin or remove the **insulating film** using the first anodic oxide film as a mask, thereby forming a gate **insulating film**;

removing the first anodic oxide film after the etching; and

introducing ions of an impurity of an N or P type conductivity into a portion of the **semiconductor** layer using the gate electrode and the gate **insulating film** as a mask,

where the introducing is carried out with at least two different conditions having a higher acceleration voltage and a lower acceleration voltage.

A method of mfg. a **semiconductor device** comprising the steps of:

forming a **semiconductor layer** on an **insulating** surface;

forming an **insulating film** on an entire surface of the **semiconductor** layer;

forming a gate electrode on the **insulating film**;

patterning the **insulating film** into a gate **insulating film** in such a manner that the gate **insulating film** extends beyond side edges of the gate electrode but does not completely cover the **semiconductor** layer so that portions of the **semiconductor** layer are exposed; and

introducing one conductivity type impurity ions into the **semiconductor** layer using the gate electrode and the gate **insulating layer** as a mask,

where a condition of the introducing step is selected so that regions of the **semiconductor** layer located below extensions of the gate **insulating film** beyond the gate electrode are

added with the impurity at a first concentration while exposed regions of the **semiconductor** layer are added with the impurity at a second concentration which is different from the first concentration,

where the **insulating film** is patterned by using a mask which is an anodic oxide film formed on side surfaces of the gate electrode.

Dwg.0/7

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013013281
WPI Acc No: 2000-185132/200017
Related WPI Acc No: 1995-202132; 1996-430739
XRAM Acc No: C00-058210
XRPX Acc No: N00-136754

Manufacture of **thin film transistors** for liquid crystal device, comprises crystalline silicon **semiconductor** layer which has been heat crystallized at a relatively low temperature because of the use of a crystallisation promoting material

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: MIYANAGA A; OHTANI H; TAKEYAMA J
Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 984317	A2	20000308	EP 94308974	A	19941202	200017	B
			EP 99121017	A	19941202		

Priority Applications (No Type Date): JP 93339397 A 19931202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 984317	A2	E	23	G02F-001/1368	Div ex application EP 94308974 Div ex patent EP 656644

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 984317 A2
Abstract (Basic):

NOVELTY - An active matrix display device comprises a crystalline silicon **semiconductor** layer which has been heat crystallized at a relatively low temperature because of the use of a crystallisation promoting material such as Ni, Pd, Pt, Cu, Ag, Au, In, Sn, **Pb**, P, As, And Sb. This material is introduced by mixing it within a liquid precursor material for forming **silicon oxide** and coating the precursor material onto the amorphous silicon film.

DETAILED DESCRIPTION - An active matrix display device comprises:

(a) a **semiconductor** layer with first and second impurity regions and a channel formation region formed on an insulating surface;

(b) a gate **insulating film** adjacent the channel formation region;

(c) a gate electrode adjacent the gate **insulating film**;

(d) an **insulating film** (215) comprising an organic resin formed over the previous layers;

(e) a pixel electrode (216) formed on the **insulating film** and electrically connected to one of the first and second impurity regions; and

(f) a conductive **layer** formed on the **insulating film** and electrically connected to the other one of the first and second impurity regions.

An INDEPENDENT CLAIM is also included for an active matrix display device comprising a glass substrate, a blocking film and a similar

structure as above.
Preferably, the display device is a liquid crystal device.
USE - Manufacture of **thin film transistors** for integrated circuits, e.g. as switching elements in an active **matrix circuit** in an electro-optical device or as a driving circuit formed on the same substrate as the active **matrix circuit**.
ADVANTAGE - The concentration of catalyst for promoting the crystallisation can be accurately controlled and minimized.
DESCRIPTION OF DRAWING(S) - The drawing illustrates a process step for manufacturing a **thin film transistor** according to the invention.
Interlayer **insulating film** (214)
Transparent polyimide film (215)
Pixel electrode (216)
Electrode/wirings (217,218)
pp; 23 DwgNo 6F/8

42/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010037281
WPI Acc No: 1994-304992/199438
XRAM Acc No: C94-138995
XRPX Acc No: N94-239841
Thin film transistor mfr. - using three or four mask levels, esp. for flat LCD screen prodn
Patent Assignee: THOMSON-LCD (CSFC)
Inventor: HEPP B; SANSON E; SZYDLO N
Number of Countries: 019 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2702882	A1	19940923	FR 933012	A	19930316	199438	B
WO 9421102	A2	19940929	WO 94FR278	A	19940315	199439	
EP 689721	A1	19960103	EP 94909965	A	19940315	199606	
			WO 94FR278	A	19940315		
WO 9421102	A3	19941110	WO 94FR278	A	19940315	199610	
JP 9506738	W	19970630	JP 94520709	A	19940315	199736	
			WO 94FR278	A	19940315		
US 5830785	A	19981103	WO 94FR278	A	19940315	199851	
			US 96522243	A	19960222		

Priority Applications (No Type Date): FR 933012 A 19930316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2702882	A1		26	H01L-021/336	
WO 9421102	A2	F	24	H01L-021/00	
Designated States (National): JP KR US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 689721	A1	F		H01L-027/12	Based on patent WO 9421102
Designated States (Regional): DE FR GB NL					
JP 9506738	W		29	H01L-029/786	Based on patent WO 9421102
US 5830785	A			H01L-021/00	Based on patent WO 9421102
WO 9421102	A3			H01L-021/336	

Abstract (Basic): FR 2702882 A

A mfg. process for direct staged (gate above source and drain) TFTs with four mask levels involves (a) depositing and etching a first conductor level on an insulating substrate to form a source (1) and drain (2); (b) depositing and etching a **semiconductor** level alone or followed by a **first insulation** level joining the source and drain; (c) depositing and etching a **second insulation** level; and (d) depositing and etching a second conductor level (15) to form the gate of the transistor (20).

A similar process with three mask levels involves carrying out step (a); depositing a **semiconductor** level and an insulation level and etching both levels joining the source and drain; oxidising, nitriding or passivating the **semiconductor** level sidewalls; and depositing and etching a conductor level (15).

Also claimed are (i) a liq. crystal screen including an active **matrix**, the **pixel electrode**-driving active elements

of which are TFTs made by the above processes; (ii) a liq. crystal screen including an active matrix and an integrated driver, the active elements driving the pixel electrodes and forming the integrated driver being TFTs made by the above processes; and (iii) an electronic circuit on an insulating substrate, made by the above processes.

The substrate is pref. a glass sheet. The conductive materials are Al, **Ti**, Cr, Mo, **W**, **Ta**, ITO, alloys or multilayers, the first conductive level pref. being of transparent ITO or SnO2. The **semiconductor** is a-Si:H, polysilicon or microcrystalline Si. The insulating material is **silicon dioxide**, **nitride** or **oxynitride**.

USE - In mfr. of flat LCD screens, esp. with integrated drivers.

ADVANTAGE - The processes allow passivation of the transistors during mfr., to make them insensitive to light from above, and allow connection of the gate of one transistor to the source or drain of the same or another transistor.

Dwg.1d/3

2/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05859536

ACTIVE **MATRIX** TYPE DISPLAY **CIRCUIT**

PUB. NO.: 10-142636 [JP 10142636 A]
PUBLISHED: May 29, 1998 (19980529)
INVENTOR(s): TAKEMURA YASUHIKO
YAMAZAKI SHUNPEI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-310033 [JP 96310033]
FILED: November 06, 1996 (19961106)

ABSTRACT

PROBLEM TO BE SOLVED: To increase the auxiliary capacity without reducing the numerical aperture by using a **semiconductor** layer or wiring and a conductive film used as black **matrix** as **electrodes**, and using a silicon nitride as dielectric to form the auxiliary capacity.

SOLUTION: A gate wiring 2 and a capacity wiring 3 are formed on a glass substrate 1 having a silicon nitride film formed as bed film. A **silicon oxide** film 4 is formed as gate **insulating film** , and an amorphous silicon film is formed. The amorphous silicon film is etched to provide a **semiconductor** layer 5 of **thin film transistor**. A polycrystalline silicon film having phosphor is formed and etched to provide a source 6 and a drain 7. Further, a data wiring 8 is provided by use of an aluminum film. A first auxiliary capacity 9 having the gate **insulating film** 3 as **dielectric** is formed between the capacity wiring 3 and the drain 7. A silicon nitride film 10 is then formed, and a polyimide layer 11 is form followed by etching to form the hole 12 of the auxiliary capacity. A **titanium** film is etched to form a black matrix.

44/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007573122
WPI Acc No: 1988-207054/198830
XRPX Acc No: N88-157845
LCD with electrodes with associated transistor - has transistors selected for same light transmission voltage characteristic for each colour
Patent Assignee: HOSIDEN ELECTRONICS CO LTD (HOSD); HOSHI DENKI SEIZO KK (HOSD); HOSIDEN ELTRN CO LTD (HOSD); HOSIDEN CORP (HOSD)
Inventor: UKAI Y
Number of Countries: 015 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 276001	A	19880727	EP 88100843	A	19880121	198830	B
JP 63180936	A	19880726	JP 8713171	A	19870122	198835	
US 4810060	A	19890307	US 88143863	A	19880114	198912	
EP 276001	B1	19960403	EP 88100843	A	19880121	199618	
DE 3855168	G	19960509	DE 3855168	A	19880121	199624	
			EP 88100843	A	19880121		

Priority Applications (No Type Date): JP 8713171 A 19870122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 276001	A	E	7		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 4810060	A		7		
EP 276001	B1	E	10	G02F-001/133	
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
DE 3855168	G			G02F-001/133	Based on patent EP 276001

Abstract (Basic): EP 276001 A
The active colour liq. crystal display has a **matrix** of display **electrodes** (15) which have apposed colour filters and are connected to respective **thin film transistors** controlled by the input colour image signal. To provide the same light transmission voltage characteristic for all three colour filter regions, the transistors associated with the three regions are selected to have an approp. different channel configuration.
The gate **insulating film** thickness, **semiconductor layer impurity concentration**, or storage capacitance are also made different by inclusion of an auxiliary capacitor (34) in parallel with the display electrode.
ADVANTAGE - Eliminates variation of contrast with colour
Abstract (Equivalent): EP 276001 B
An active colour liquid crystal display device comprising: first and second substrates (11, 12) arranged substantially parallel and mutually opposed; a liquid crystal material (14) confined between said first and second substrates (11, 12); display **electrodes** (15) arranged in **matrix** form together with corresponding **thin film transistors** (16) and address circuitry deposited on the inner surface of said first substrate (11); a common electrode (17) deposited on the inner surface of said second substrate (12); colour

filters (1B, 1G, 1B) of three primary colours arranged in matrix form substantially opposite said display electrodes (15), each colour filter and corresponding display electrode (15) forming a colour element; characterised in that the ratio between the width (W), and length (L) of the current channel of each **thin film transistor** or the thickness of the gate **insulating film** (22) of each **thin film transistor** or the **impurity concentration** of the **semiconductor** layer (21) of each **thin film transistor** is selected in accordance with the colour filter of the corresponding colour element so that the characteristic of light transmission versus applied gate voltage is substantially the same for all of said colour elements.

(Dwg.6/7

Abstract (Equivalent): US 4810060 A

The active colour liquid crystal display element has display **electrodes** arranged in a **matrix** form within a liquid crystal cell. Colour filters of three primary colours are each disposed opposite one of the display electrodes, and are distributed uniformly. A **thin film transistor** is connected to each display electrode and is controlled, by switching, in accordance with an input colour image siqnal to charge and discharge the display electrode for displaying a colour image.

The structures of the **thin film transistors** are selected corresponding to the colour filters of the three primary colours so that the same light transmission-voltage characteristic is provided for all the three colour filter portions.

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012754301
WPI Acc No: 1999-560418/199947
XRAM Acc No: C99-163272
XRPX Acc No: N99-413982
Liquid crystal display apparatus for portable computers
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: AKIYAMA M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5952991	A	19990914	US 96748897	A	19961114	199947	B

Priority Applications (No Type Date): US 96748897 A 19961114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5952991	A		26	G09G-003/36	

Abstract (Basic): US 5952991 A
Abstract (Basic):

NOVELTY - Since the liquid crystal display of the invention comprises a number of voltage applying means (including drive circuits) for driving the liquid crystal, and a controlling means for switching the voltage means from one to another, the controlling means having the switched state, a number of display modes can be selected. With a display mode having a **low** driving frequency the **power** consumption is markedly reduced. In the display mode a gradation driving mode with high picture quality can be selected.

DETAILED DESCRIPTION - (A) Liquid crystal display apparatus comprising; (i) Means of applying a first voltage at a first frequency to a liquid crystal and having at least one nonlinear switching element and intersecting a scanning line so as to form a matrix. (ii) Means of applying a second voltage at a second and lower frequency to a liquid crystal and having at least one nonlinear switching element. (iii) Means for controlling the voltage alternately and having a memory portion for storing a switched state for switching between a sampling and a selected state, where the sampling state samples the first voltage at a sampling time and consequently applies a sampling voltage corresponding to the first voltage to the liquid crystal, and the selected state selects the second voltage. INDEPENDENT CLAIM - (B) Also included is the display as (A) in which the **matrix** is a **matrix** of **pixels electrodes** each having first, second, and memory portions, and first and second signal lines supply voltage to the pixels. A number of scanning lines intersect the first signal line. The first circuit samples a the first voltage and applies it to the pixel electrode, the second circuit is connected to the second signal line and the memory portion, selects a voltage applied to the second signal line and applies it to the pixel electrode. The memory portion stores a switched state by a signal supplied from the first circuit and switches alternately between a sampling state and a selected state.

USE - Active matrix liquid crystal displays for portable computers etc.

ADVANTAGE - The apparatus has a marked reduction in power consumption of the drive circuit without affecting display quality.

DESCRIPTION OF DRAWING(S) - The drawing shows a pixel of a liquid crystal display.

pp; 26 DwgNo 1A/22

48/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011127901
WPI Acc No: 1997-105825/199710
XRAM Acc No: C97-033876
XRPX Acc No: N97-087628
Thin film **semiconductor device** mfr. using laser annealing technique for LCD - involves controlling width of slope part of trapezoidal distribution in direction of X-axis to less than or equal to 100 micrometers
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8340118	A	19961224	JP 95168098	A	19950609	199710	B

Priority Applications (No Type Date): JP 95168098 A 19950609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8340118	A		6	H01L-029/786	

Abstract (Basic): JP 8340118 A

The mfg method involves forming a mono crystal type **semiconductor** thin **film** (13) on an **insulated** substrate (1). A laser beam (4) is irradiated on the **semiconductor** thin film for crystallising the **semiconductor** thin film. The irradiation direction of the laser beam is made to overlap the direction of X-axis partially during the irradiation. The **semiconductor** thin film is crystallised by irradiating the laser beam intermittently.

The intensity distribution of the laser beam has a trapezoidal shape in the direction of X-axis. The width (S) of a slope part (7) of the trapezoidal distribution in the direction of X-axis is controlled to have value less than or equal to 100micrometers. The width (**W**) of a strip shaped part (8) is controlled to have a value less than or equal to 7micrometers.

ADVANTAGE - Reduces formation of uneven strip shaped part. Stabilises switching of **pixel electrode** in active **matrix** type display device.

Dwg.1/6

48/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010067198
WPI Acc No: 1994-334911/199442
XRPX Acc No: N94-263013
Thin film transistor for **pixel electrode** switching in active **matrix** LCD - has microcrystalline silicon contact layers, with less tan 10 ohm-cm resistivity, overlying gate electrode, with source and drain electrodes contacted to contact layers and e.g. offset w.r.t. each other
Patent Assignee: SHARP KK (SHAF)
Inventor: KATAYAMA M; KAWAI K
Number of Countries: 007 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 622855	A2	19941102	EP 94303130	A	19940429	199442	B
JP 6314788	A	19941108	JP 93127838	A	19930430	199504	
JP 6314789	A	19941108	JP 93104842	A	19930430	199504	
US 5473168	A	19951205	US 94233805	A	19940426	199603	
EP 622855	A3	19960417				199626	
KR 159318	B1	19981201	KR 949370	A	19940429	200032	
JP 3129878	B2	20010131	JP 93127838	A	19930430	200109	
EP 622855	B1	20010627	EP 94303130	A	19940429	200137	
DE 69427556	E	20010802	DE 627556	A	19940429	200151	
			EP 94303130	A	19940429		

Priority Applications (No Type Date): JP 93127838 A 19930430; JP 93104842 A 19930430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 622855	A2	E	55	H01L-029/784	
Designated States (Regional): DE FR GB NL					
JP 6314788	A		11	H01L-029/784	
JP 6314789	A		10	H01L-029/784	
US 5473168	A		32	H01L-029/78	
KR 159318	B1			H01L-029/786	
JP 3129878	B2		11	H01L-029/786	Previous Publ. patent JP 6314788
EP 622855	B1	E		H01L-029/772	
Designated States (Regional): DE FR GB NL					
DE 69427556	E			H01L-029/772	Based on patent EP 622855

Abstract (Basic): EP 622855 A

The **TFT** includes a **semiconductor** layer formed on a substrate over, and insulated from, a gate electrode on the substrate. There are two contact layers, made of n-type microcrystalline silicon with a 10 Omega cm or less resistivity, in contact with the **semiconductor** layer and over the gate electrode. Source and drain electrodes each respectively contact one of the contact layers. Pref. one or both of the source-drain layers don not overlap the gate electrode

The source and drain electrodes may be formed directly on the

substrate, with the corresp. contact layers partly covering the electrodes. The source-drain electrode width in the channel width direction is pref. less than the contact layer width e.g. by at least 3 mu m.

ADVANTAGE - Reduced transistor size, with reduced pattern margins; e.g. reduced parasitic capacitance.

Dwg.2/50

Abstract (Equivalent): US 5473168 A

What is claimed is:

1. A **thin film transistor** comprising:

a substrate;

a gate electrode formed on said substrate;

a **semiconductor layer insulated** from said gate electrode, said **semiconductor** layer being formed above said substrate to cover said gate electrode;

a first contact layer and a second contact layer which are made of n-type microcrystalline silicon having a resistivity of 10 omegacm of less, each of said first and second contact layers having a top surface and a bottom surface, one of the top surface and the bottom surface being in contact with said **semiconductor** layer to cover part of said gate electrode, an outer edge of each of the first and second contact layers being in alignment with an outer edge of the **semiconductor** layer;

a source electrode which is in contact with part of the other of the top surface and the bottom surface of said first contact layer; and

a drain electrode which is in contact with part of the other of the top surface and the bottom surface of said second contact layer,

wherein at least one of said source and drain electrodes is disposed not to overlap said gate electrode,

wherein a width in a channel width direction of at least one of said source and drain electrodes is smaller than a width in the channel width direction of said first and second contact layers, and

wherein said width in the channel width direction of said at least one of said source and drain electrodes is determined so that an end of said at least one of said source and drain electrodes is located apart from an end of a corresponding one of said first and second contact layers by a distance of 3 mum or more.

(Dwg.11/50

48/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009067858
WPI Acc No: 1992-195257/199224
XRAM Acc No: C93-012241
XRPX Acc No: N93-020897
Thin-film transistor for liq. crystal display device - has gate electrode structure of **tantalum** film covered with aluminium@ film with aluminium oxide as gate insulation
Patent Assignee: HITACHI LTD (HITA)
Inventor: MATSUKAWA Y; MATSUMARU H; SASANO A; SHIRAHASHI K; TANIGUCHI H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 4065168	A	19920302	JP 90176352	A	19900705	199224	B
US 5177577	A	19930105	US 91726404	A	19910705	199304	
KR 209471	B1	19990715	KR 9111377	A	19910705	200102	

Priority Applications (No Type Date): JP 90176352 A 19900705
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 4065168	A		19	H01L-029/784	
US 5177577	A		26	H01L-027/01	
KR 209471	B1			H01L-029/78	

Abstract (Basic): JP 4065168 A

Thin-film transistor comprises: substrate; gate electrode formed of a first level **Ta** film and a second level Al **film**; gate **insulation** comprising oxidised Al; **semiconductor** film; and source and drain electrodes. Pref. the gate insulaton further includes Si nitride on the oxidised (anodised) Al and the **semiconductor** is Si.

USE/ADVANTAGE - In a liq. crystal display **circuit** of active **matrix** type (claimed). To provides excellent adhesion to the (glass) substrate while the Al oxide provides a high breakdown voltage. (First major country equivalent to J04065168-A)

US 5177577 A

Thin-film transistor comprises: substrate; gate electrode formed of a first level **Ta** film and a second level Al **film**; gate **insulation** comprising oxidised Al; **semiconductor** film; and source and drain electrodes. Pref. the gate insulaton further includes Si nitride on the oxidised (anodised) Al and the **semiconductor** is Si.

USE/ADVANTAGE - In a liq. crystal display **circuit** of active **matrix** type (claimed). To provides excellent adhesion to the (glass) substrate while the Al oxide provides a high breakdown voltage. (First major country equivalent to J04065168-A)

Dwg.0/0

48/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009033400
WPI Acc No: 1992-160756/199220
XRAM Acc No: C92-074153
XRPX Acc No: N92-120558
Active **matrix** substrate with short-**circuit** prevention insulation - gives higher display quality in LCD(s), and reduces number of defects
Patent Assignee: SEIKO EPSON CORP (SHIH)
Inventor: HIDETO I; NAKAZAWA T; ISHIGURO H
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 484965	A	19920513	EP 91119064	A	19911108	199220	B
JP 5027266	A	19930205	JP 91253733	A	19911001	199310	
EP 484965	A3	19931201	EP 91119064	A	19911108	199513	
US 5614730	A	19970325	US 91790253	A	19911108	199718	

Priority Applications (No Type Date): JP 91253733 A 19911001; JP 90305069 A 19901109; JP 90315424 A 19901120; JP 90315426 A 19901120; JP 90318810 A 19901122; JP 9176404 A 19910409; JP 91101246 A 19910507; JP 91104244 A 19910509; JP 91105768 A 19910510
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 484965	A	E	48		
Designated States (Regional): DE FR GB NL					
JP 5027266	A		19	G02F-001/136	
US 5614730	A		43	H01L-029/04	

Abstract (Basic): EP 484965 A
(+20.11.90(2), 22.11.90, 9.4.91, 7.5.91, 9.5.91, 10.5.91 -JP-315424/6, 318810, 076404, 101246, 104244, 105768) Active matrix substrate, which has a **multilayer insulator** to prevent short circuits between data bus and picture element electrode or scanning line, comprises a **thin film transistor** on a substrate with a scanning line (101) connected to its gate, a data bus (108) to its source, and a pixel electrode connected to the data bus through the **TFT**. The active matrix substrate comprises the scanning line with its surface covered by an **insulating film** (112), and a **semiconductor** layer covered with a gate **insulating film** (111) comprising the **TFT**.

Also claimed is an active matrix substrate as above, specifying that the scanning line is capacity-coupled to the gate electrode of the **TFT**.

USE/ADVANTAGE - Active matrix substrate is used for LCDs, image sensors, three-dimensional ICs etc. Short-circuits caused by defective photoresists and gate insulation pinholes are eliminated, giving higher display quality and less need for defect inspection. Also the scanning line and gate electrode may be optimised separately and the d.c. charge to the liq. crystal layer is reduced.

Dwg.1C/28

Abstract (Equivalent): US 5614730 A

A liq. crystal device, comprising: a pair of opposed and spaced apart insulating substrates; a number of scanning lines and a number of data lines disposed on one of the substrates, the scanning lines intersecting the data lines at cross-over locations; a number of switching elements connected to the scanning lines and the data lines; pixel electrodes arranged on the one of the substrates, each of the pixel electrodes being electrically connected to respective ones of the switching elements and being extended so as to overlap one of the scanning lines connected to an adjacent one of the switching elements; a number of first layers located between each of the scanning lines and each of the data lines at the cross-over locations, the number of first layers including a first electrically conductive film, a **tantalum** oxide **film** and an electrically **insulating film**; and a number of second layers located between each of the pixel electrodes and each of the scanning lines, the number of second layers including a number of electrically **insulating films** and a second electrically conductive film.

Dwg.19a/26

48/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008971139
WPI Acc No: 1992-098408/199213
Related WPI Acc No: 1991-319209; 1993-160772
XRAM Acc No: C92-045657
XRPX Acc No: N92-073671
Thin film transistor suitable for LC matrix display - has gate electrode formed of **titanium**@-contg. aluminium@ to provide reduced contact resistance
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: ISHII H; KONYA N; MATSUDA K; MORI H; OHNO I; ; SATO S; SHIOTA J
Number of Countries: 007 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 476701	A	19920325	EP 91116062	A	19910920	199213	B
JP 4130776	A	19920501	JP 90250381	A	19900921	199230	
JP 4130777	A	19920501	JP 90250383	A	19900921	199230	
JP 4299865	A	19921023	JP 9187248	A	19910328	199249	
EP 476701	A3	19920415	EP 91116062	A	19910920	199328	
US 5243202	A	19930907	US 91690816	A	19910423	199337	
			US 91762937	A	19910919		
			US 934641	A	19930112		
US 5367179	A	19941122	US 91690816	A	19910423	199501	
			US 91762937	A	19910919		
			US 92975282	A	19921112		
EP 476701	B1	19951213	EP 91116062	A	19910920	199603	
DE 69115405	E	19960125	DE 615405	A	19910920	199609	
			EP 91116062	A	19910920		

Priority Applications (No Type Date): JP 9187248 A 19910328; JP 90250381 A 19900921; JP 90250383 A 19900921; JP 90107376 A 19900425; JP 90107377 A 19900425; JP 90235675 A 19900907; JP 90239940 A 19900912; JP 90239941 A 19900912; JP 90242576 A 19900914; JP 90242577 A 19900914; JP 91326773 A 19911115; JP 91326774 A 19911115; JP 91326775 A 19911115; JP 91326777 A 19911115; JP 91355633 A 19911224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 476701	A		58		
Designated States (Regional): DE FR GB IT NL					
JP 4130776	A		14	H01L-029/784	
JP 4130777	A		10	H01L-029/784	
JP 4299865	A		6	H01L-029/784	
US 5243202	A		46	H01L-027/01	CIP of application US 91690816 Cont of application US 91762937
US 5367179	A		14	H01L-023/48	CIP of application US 91690816 CIP of application US 91762937 CIP of patent US 5284789
EP 476701	B1	E	58	H01L-029/772	
Designated States (Regional): DE FR GB IT NL					
DE 69115405	E			H01L-029/772	Based on patent EP 476701

Abstract (Basic): EP 476701 A

A **thin film transistor** (**TFT**) comprises (a) an insulating substrate (101); (b) a non-monocrystalline Si **semiconductor** film (114) placed above the substrate; (c) an **insulating film** (113) placed on the **semiconductor** film; (d) a pair of first electrodes (116, 117), spaced a specified distance apart in a plane and electrically connected to the **semiconductor** film so as to form the channel region of the transistor; and (e) a second electrode (112) placed so as to sandwich the **insulating film** between itself and pair of first electrodes. The electrode, or electrode pair formed on the substrate is made of **titanium**-contg. aluminium.

USE/ADVANTAGE - **TFT** is used in active-matrix LCD's. The use of an amt. of **Ti** in the Al comprising the electrodes reduces the electrodes resistance. Hence stable operation of a LCD is assured by lowering resistance of electrodes, scanning signal lines and/or the data signal lines without causing defects in the gate **insulating films**.

Dwg.7/3b

Abstract (Equivalent): EP 476701 B

A **thin-film transistor** which comprises an insulating substrate (101) a non-single-crystal silicon **semiconductor** film (14) placed above said substrate, an **insulating film** (113) placed on said **semiconductor** film, and a pair of first electrodes (116) spaced a specified distance apart in a plane and electrically connected to said **semiconductor** film so as to form the channel region of the transistor, and a second electrode (112) placed so as to sandwich at least said **insulating film** between itself and said pair of first electrodes, of said first electrode pair and said second electrode, at least the electrode or electrode pair formed on said substrate being made of **titanium** -containing aluminium, characterised in that said **titanium** -containing aluminium has a **titanium** content of 2.2% or more by weight.

Dwg.7/36

Abstract (Equivalent): US 5243202 A

Thin film transistor comprises an **insulating** substrate (eg glass) on which is mounted a silicon **semiconductor** film (not a single crystal type), then an **insulating film** (eg a single Si3N4 layer or a composite of Si3N4 and La2O3 layers), with two electrodes connected to the **semiconductor** film to stand astride a transistor channel region; and a third electrode is mounted on the substrate to sandwich the **insulating layer** between itself and the two **semiconductor** electrodes; such that the third electrode and/or the other two electrodes are **Ti**-Al alloy electrodes.

USE - The prods. are gate **electrodes** for liq. crystal **matrix** display devices.

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48/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008815196
WPI Acc No: 1991-319209/199144
Related WPI Acc No: 1992-098408; 1993-160772
XRAM Acc No: C91-137933
XRPX Acc No: N91-244693
Deposition of silicon-based films - by RF glow discharge at controlled substrate temp. and RF power density
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: KONYA N; MORI H; SATO S; ISHII H; MATSUDA K; OHNO I; SHIOTA J
Number of Countries: 008 Number of Patents: 018
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 454100	A	19911030	EP 91106621	A	19910424	199144	B
JP 4006820	A	19920110	JP 90107377	A	19900425	199208	
JP 4006834	A	19920110	JP 90107376	A	19900425	199208	
JP 4116826	A	19920417	JP 90235675	A	19900907	199222	
JP 4120733	A	19920421	JP 90239940	A	19900912	199222	
JP 4120737	A	19920421	JP 90239941	A	19900912	199222	
JP 4123423	A	19920423	JP 90242576	A	19900914	199223	
JP 4123424	A	19920423	JP 90242577	A	19900914	199223	
EP 454100	A3	19920304	EP 91106621	A	19910424	199325	
US 5243202	A	19930907	US 91690816	A	19910423	199337	
			US 91762937	A	19910919		
			US 934641	A	19930112		
US 5284789	A	19940208	US 91690816	A	19910423	199407	
US 5367179	A	19941122	US 91690816	A	19910423	199501	
			US 91762937	A	19910919		
			US 92975282	A	19921112		
KR 9408356	B1	19940912	KR 916715	A	19910425	199633	
EP 454100	B1	19971119	EP 91106621	A	19910424	199751	
DE 69128210	E	19980102	DE 628210	A	19910424	199806	
			EP 91106621	A	19910424		
JP 2727532	B2	19980311	JP 90242577	A	19900914	199815	
JP 2732543	B2	19980330	JP 90242576	A	19900914	199818	
JP 2900284	B2	19990602	JP 90239940	A	19900912	199927	

Priority Applications (No Type Date): JP 90242577 A 19900914; JP 90107376 A 19900425; JP 90107377 A 19900425; JP 90235675 A 19900907; JP 90239940 A 19900912; JP 90239941 A 19900912; JP 90242576 A 19900914; JP 90250381 A 19900921; JP 90250383 A 19900921; JP 9187248 A 19910328; JP 91326773 A 19911115; JP 91326774 A 19911115; JP 91326775 A 19911115; JP 91326777 A 19911115; JP 91355633 A 19911224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 454100	A		34		
Designated States (Regional): DE FR GB IT NL					
JP 4116826	A		6	H01L-021/318	
JP 4120733	A		7	H01L-021/318	
JP 4120737	A		9	H01L-021/336	

JP 4123423	A	6	H01L-021/205	
JP 4123424	A	7	H01L-021/205	
EP 454100	A3	34		
US 5243202	A	46	H01L-027/01	CIP of application US 91690816 Cont of application US 91762937
US 5284789	A	30	H01L-021/00	
US 5367179	A	14	H01L-023/48	CIP of application US 91690816 CIP of application US 91762937 CIP of patent US 5284789
EP 454100	B1 E	34	H01L-021/318	
Designated States (Regional): DE FR GB IT NL				
DE 69128210	E		H01L-021/318	Based on patent EP 454100
JP 2727532	B2	6	H01L-021/205	Previous Publ. patent JP 4123424
JP 2732543	B2	6	H01L-021/205	Previous Publ. patent JP 4123423
JP 2900284	B2	5	H01L-021/336	Previous Publ. patent JP 4120733
KR 9408356	B1		H01L-021/203	

Abstract (Basic): EP 454100 A

Thin film of Si-contg. material is deposited by RF glow discharge with a substrate temp. of 230-270 deg.C and an RF power of 60-100mW/sq.cm. In an embodiment, Si3N4 is deposited from SiH4 and NH3 in an N2 carrier. Alternatively, SiO2 is deposited from SiH4 and N2O in an N2 carrier.

USE/ADVANTAGE - Esp. in mfr. of **thin-film transistors**. Dense film with a high breakdown voltage is obtd. at a relatively low temp. (34pp Dwg.No.20/27)

Abstract (Equivalent): EP 454100 B

A method of forming a silicon nitride film, comprising: locating a substrate (104) to oppose a high-frequency electrode (106) which receives a high-frequency power (111) within a hermetic chamber (101); supplying a process gas into said chamber and generating a plasma upon supply of the high-frequency power (111) to said high-frequency electrode (106); and depositing a thin film essentially consisting of silicon nitride on a surface of said substrate (104), characterised in that said substrate (104) is kept heated in a temperature range of 230 degrees C to 270 degrees C, and the high-frequency power (111) is supplied to said high-frequency electrode (106) so that the RF discharge power density falls within a range of 60 to 100 mW/cm2.

Dwg.5/21

Abstract (Equivalent): US 5243202 A

Thin film transistor comprises an **insulating** substrate (eg glass) on which is mounted a silicon **semiconductor** film (not a single crystal type), then an **insulating film** (eg a single Si3N4 layer or a composite of Si3N4 and La2O3 layers), with two electrodes connected to the **semiconductor** film to stand astride a transistor channel region; and a third electrode is mounted on the substrate to sandwich the **insulating layer** between itself and the two **semiconductor** electrodes; such that the third electrode and/or the other two electrodes are **Ti**-Al alloy electrodes.

USE - The prods. are gate **electrodes** for liq. crystal **matrix** display devices.

(Dwg.7/36)

US5284789 The thin film is formed by (a) placing a substrate in a

chamber contg. high frequency electrodes and maintaining the substrate at 230-270 deg.C, (b) supplying a carrier gas into the chamber, and adjusting the internal pressure and temp. of the chamber to predetermined levels, supplying **HF** power between the substrate and the electrodes, then supplying reaction gas after electric discharge occurs, (c) applying **HF** power having a discharge power density of 60-100 mW/cm2 to the electrodes to generate plasma, (d) maintaining the predetermined temp. of the substrate and depositing an insulator of Si-based material to a predetermined thickness while the gas and **HF** power are supplied, and (e) cooling the substrate and removing from the chamber.

The carrier gas is pref. N2 and the reaction gas is silane and NH3 or N2O.

A method of mfg. a **thin film transistor** by the above method is also claimed.

ADVANTAGE - A dense Si-based thin film with high breakdown voltage can be formed at a lower temp. than conventional processes. The obtd. **TFT** has good characteristics.

(Dwg.5/27)

US5367179 **Thin-film transistor** comprises (a) an insulating substrate; (b) a gate electrode made of aluminium alloy contg. a high m.pt. metal and 4% or more atomic O and/or N upon (a); (c) a gate **insulating film** formed on (b); (d) an i-type **semiconductor** layer upon this; and (e) a source electrode and drain electrode electrically connected to each end of (d).

Pref. (b) is made of aluminium alloy, **titanium** and oxygen, aluminium alloy, **titanium** and nitrogen, or aluminium alloy, **tantalum** and oxygen.

ADVANTAGE - Short-circuiting between conductive layers is prevented.

48/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008437731
WPI Acc No: 1990-324731/199043
XRAM Acc No: C90-140785
XRPX Acc No: N90-248429

Active **matrix circuit** substrate for image display - with supplementary path lines for path connecting gate electrodes and path connecting drain electrodes

Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2232627	A	19900914	JP 8951908	A	19890306	199043	B

Priority Applications (No Type Date): JP 8951908 A 19890306

Abstract (Basic): JP 2232627 A

Active **matrix circuit** substrate comprises individual **thin film transistors** with gate electrode, gate **insulating film**, active **layer** of **semiconductor** film, drain electrode, source electrode and display image element electrode formed on the insulating substrate. The gate . electrodes of the individual **thin film transistors** are connected with each other through a first path line as a scanning line, the drain electrodes are connected with each other through a second path line as a signal line, and a supplementary path line is put on the first- and second path line, respectively. The first supplementary path line is made of a material having a low resistance and reduced contact resistance with the first path line. The second path line is formed of the display image element electrode material, and the second supplementary path line having a film-thickness larger than that of the second path line and made of a low-resistance material.

Pref. at least one kind of material selected from the gp. consisting of **Ti**, Zr, **Hf**, V, Nb, **Ta**, Cr, Mo and **W** (nitrides) is inserted on the side where the supplementary path line is brought into contact with the first path line and the second path line.

USE/ADVANTAGE - For the active **matrix circuit** substrate the probability of breakage of the first path line as the scanning line and the second path line as the signal line can be reduced and the resistance can be reduced. (10pp Dwg.No.1/6)

48/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007103745
WPI Acc No: 1987-103742/198715
XRAM Acc No: C87-042939
XRPX Acc No: N87-077814

Liquid crystal display device - has **thin film transistor** of amorphous silicon **semiconductor** insulated from overlapping part of picture element electrode

Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 62047621	A	19870302	JP 85190852	A	19850827	198715	B

Priority Applications (No Type Date): JP 85190852 A 19850827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 62047621	A		4		

Abstract (Basic): JP 62047621 A

The device has on one of the base plates (a) a **matrix** of picture element **electrodes** composed of transparent film conductor and (b) **thin film transistor** (**TFT**) connected with each picture element electrode. The device is characterised by (1) semi-conductor film of the **TFT** is composed of amorphous silicon (a-Si); (2) the semi-conductor **film** is electrically **insulated** from the overlapping part of the picture element electrode; and (3) phosphorus-doped a-Si film layer is sandwiched between source and drain electrodes of the **TFT** and the semi-conductor film.

ADVANTAGE - By **insulating** the a-Si **layer** from the transparent conductor (e.g., ITO = indium tin oxide) layer, and sandwiching P-doped a-Si layer between the source and drain electrodes and undoped a-Si layer, the transparent conductor is protected from the reaction with the source/drain electrode material (e.g., aluminium) or/and with the undoped a-Si layer, to improve reliability of the **TFT**.

In an example, 2000 Angstrom-thick sputtered **Ta** layer is patterned by photolithography to form the gate electrode. After coating with the first Si3N4 layer, a-Si film layer is formed by plasma CVD process. The a-Si film layer is etched to leave dots, the second Si3N4 layer and ITO layer are formed by vacuum evapn. in this order. Then patterned by photolithography to form the picture element electrode of ITO. Subsequently, P-doped a-Si layer is formed by plasma CVD, and then Al-Si layer by sputtering. Finally, patterned by photolithography to form the source and drain electrodes.

0/3

48/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06180182
IMAGE SENSOR

PUB. NO.: 11-121731 [JP 11121731 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): CHIYOU KOUYUU
SAKAKURA MASAYUKI
SATOU YURIKA
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD
APPL. NO.: 09-306516 [JP 97306516]
FILED: October 20, 1997 (19971020)

ABSTRACT

PROBLEM TO BE SOLVED: To form an active image sensor at high density on a glass or quartz substrate.

SOLUTION: A selection transistor Ts comprising a **thin film transistor**, an amplifier transistor **Ta** and a reset transistor Tr are formed in a **matrix circuit**. A photodiode PD is formed on the **matrix circuit** through an **insulating layer**. A power supply line 104 is commonly used by adjacent two lines so as to decrease the number of lines per picture element. The whole transistors in a unit 100 are formed on an insular **semiconductor** thin film so as to decrease the number of contact holes per picture element.

48/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05346843
ETCHANT AND ETCHING METHOD

PUB. NO.: 08-302343 [JP 8302343 A]
PUBLISHED: November 19, 1996 (19961119)
INVENTOR(s): KONUMA TOSHIMITSU
NISHI TAKESHI
NAKAZAWA MISAKO
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-128923 [JP 95128923]
FILED: April 28, 1995 (19950428)

ABSTRACT

PURPOSE: To obtain an etchant with which etching can be performed without deposition of crystals by using an aqueous solution of **HF** and NH(sub 4)F in which the mixing ratio of **HF** to NH(sub 4)F is specified.

CONSTITUTION: **HF** is mixed with an aqueous NH(sub 4)F solution in a specified ratio to prepare an etchant having a mixing ratio satisfying the relationship: y<-2X+10 (wherein x is the content of **HF**, y is the content of NH(sub 4)F, the content of the water is 100-x-y, 0<x<=5, and 0<y<=10). A low-alkali-glass substrate containing a large amount of Al(sub 2)O(sub 3) is shrunken by annealing and subjected to, e.g. sputtering in an oxygenic atmosphere to form an SiO(sub 2) underground film. A crystalline Si film is formed by the plasma CVD method, and the substrate is etched to form a **TFT** active layer of a peripheral drive circuit and a **TFT** active layer of a **matrix circuit**. A gate **insulation film** of SiO(sub 2) is formed by sputtering in an oxygenic atmosphere, and an Al film is formed over the entire surface of the substrate by sputtering, and the substrate is etched with the etchant without forming any deposits to form a **semiconductor** circuit.

48/3,AB/11 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03473380
THIN FILM TRANSISTOR MATRIX AND MANUFACTURE THEREOF

PUB. NO.: 03-136280 [JP 3136280 A]
PUBLISHED: June 11, 1991 (19910611)
INVENTOR(s): ICHIMURA TERUHIKO
WATANABE KAZUHIRO
TAKIZAWA HIDEAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-274447 [JP 89274447]
FILED: October 20, 1989 (19891020)
JOURNAL: Section: E, Section No. 1108, Vol. 15, No. 351, Pg. 102, September 05, 1991 (19910905)

ABSTRACT

PURPOSE: To obtain a **thin film transistor** matrix which can be protected against shortcircuit defect without increasing it in manufacturing cost by a method wherein a gate electrode is formed of a bulb metal film whose surface is covered with a nitride film which is formed by nitrogenizing a base material.

CONSTITUTION: A gate electrode G, a gate **insulating film** 3, an action **semiconductor** layer 4, a source electrode S, and a drain electrode D are laminated on a transparent insulating substrate 1 in this sequence to constitute a **thin film transistor**, and the **thin film transistors** concerned are arranged in matrix to constitute a **thin film transistor matrix**, where the gate **electrode** G is formed of a bulb metal film 10 whose surface is covered with a nitride film 11 which is formed by nitrogenizing base material. For instance, a **Ti** film 10 is formed on a glass substrate 1 as thick as 80nm or so through a sputtering method, which is formed into a pattern of the gate electrode G and a bus line by removing the disused part of the film 10. Then, the surface of the **Ti** film 10 of a base material is nitrogenized in a atmosphere of N(sub 2) or NH(sub 3) at a temperature of 400 deg.C or so to form a TiN film 11 as thick as 40nm or so.

50/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012289787
WPI Acc No: 1999-095893/199908
XRPX Acc No: N99-069665
Two-terminal active wire **electrode** structure for active **matrix** liquid crystal display - has wire placed in grooves in transparent substrate and covered by **insulating layer** and-or **semiconductor** layer
Patent Assignee: GL DISPLAYS INC (GLDI-N)
Inventor: GE S; GE Y
Number of Countries: 082 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9900695	A1	19990107	WO 98US11152	A	19980603	199908	B
US 5892558	A	19990406	US 97883117	A	19970626	199921	
AU 9878057	A	19990119	AU 9878057	A	19980603	199922	
EP 991975	A1	20000412	EP 98926157	A	19980603	200023	
			WO 98US11152	A	19980603		
JP 2002513513	W	20020508	WO 98US11152	A	19980603	200234	
			JP 99505540	A	19980603		

Priority Applications (No Type Date): US 97883117 A 19970626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9900695	A1	E	35	G02F-001/133	
	Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW				
US 5892558	A			G02F-001/136	
AU 9878057	A				Based on patent WO 9900695
EP 991975	A1	E		G02F-001/133	Based on patent WO 9900695
	Designated States (Regional): DE FR GB IT				
JP 2002513513	W		39	H01L-049/02	Based on patent WO 9900695

Abstract (Basic): WO 9900695 A
The electrode structure comprises at least one conductive wire (30) having a **semiconductor** and-or **insulating layer** (32) over it. The wire and/or layer are attached to a transparent substrate (34). The wire is preferably attached to the substrate by means of an ultraviolet cured adhesive. The substrate defines grooves (38) into which the wire is placed. An array of separated electrodes (40) is formed on the substrate. The conductive wire, the layer(s) and the electrodes form an array of diodes connected in parallel. A first voltage is applied across the conductive wire and the electrodes to turn on the diodes, and a second voltage is applied across the wire and the electrodes to turn off the diodes. Preferably, the substrate comprises glass or plastic. Preferably, the wire includes

tantalum or chromium, and the **insulating layer** and/or **semiconductor** layer comprises **tantalum** oxide, or silicon nitride or organic layer. Preferably, the electrodes comprise transparent indium-tin-oxide, **tantalum** or chromium.

ADVANTAGE - Enables large screen display to be made at reasonable cost.

50/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009357021
WPI Acc No: 1993-050500/199306
XRPX Acc No: N93-203212
Semiconductor memory circuit esp. for DRAM - has level difference between wiring layers formed over gate electrodes of memory cell array selection transistor MISFET and peripheral circuit MISFET and formed in same conductor layer limited to less than 1.5~um
Patent Assignee: HITACHI DEVICE ENG CO LTD (HISD); HITACHI KEISOKU KK (HITA-N); HITACHI LTD (HITA)
Inventor: ASAYAMA K; ENDO K; KANEKO Y; MIYAZAWA H; NAGAO M; OGISHIMA A; SOEDA H; SUWANAI N; UCHIYAMA H; WATANABE K; YONEOKA T
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 5003301	A	19930108	JP 91310425	A	19911126	199306	B
US 5237187	A	19930817	US 91799541	A	19911127	199334	
US 5389558	A	19950214	US 91799541	A	19911127	199512	
			US 93104014	A	19930810		
US 5631182	A	19970520	US 91799541	A	19911127	199726	
			US 93104014	A	19930810		
			US 94327861	A	19941018		
US 6043118	A	20000328	US 91799541	A	19911127	200023	
			US 93104014	A	19930810		
			US 94327861	A	19941018		
			US 97800018	A	19970213		
KR 249268	B1	20000315	KR 9121392	A	19911127	200122	

Priority Applications (No Type Date): JP 90329122 A 19901130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 5003301	A		20	H01L-027/108	
US 5237187	A		32	H01L-027/02	
US 5389558	A		32	H01L-021/70	Div ex application US 91799541
					Div ex patent US 5237187
US 5631182	A		31	H01L-021/8242	Div ex application US 91799541
					Div ex application US 93104014
					Div ex patent US 5237187
					Div ex patent US 5389558
US 6043118	A			H01L-021/8242	Div ex application US 91799541
					Div ex application US 93104014
					Cont of application US 94327861
					Div ex patent US 5237187
					Div ex patent US 5389558
					Cont of patent US 5631182
KR 249268	B1			H01L-027/10	

Abstract (Basic): US 5237187 A
The **semiconductor** memory circuit has each memory cell constituted by a series circuit of a memory cell selecting MISFET and an information storage stacked capacitor. In a memory cell array

region, ther is a MISFET with a gate electrode and source and drain regions, two capacitor electrodes and a **dielectric film** extended over a **first insulating film** and over the gate electrode, a **second insulating film** located on the second capacitor electrode and a third **insulating film** located between the **first insulating film** and first capacitor electrode; and a first wiring positioned on the **second insulating film**.

In a peripheral circuit region, there is a second MISFET with a gate electrode and source and drain regions, a **first insulating film** on the gate electrode; a **second insulating film** on a third **insulating film**, the third **insulating film** located between the first and **second insulating films**, and a second wiring on the **second insulating film**. The second wiring is formed by the same level conductor layer as that forming the first wiring. Similarly, the first through third **insulating films** of the first region are correspondingly associated with the first through third **insulating films** of the second region, respectively.

USE/ADVANTAGE - Also suitable for SRAM. Improved integration density, product yield and reliability.

Dwg.1/20

Abstract (Equivalent): US 5631182 A

A method for fabricating a **semiconductor** memory circuit device having an array of memory cells arranged in a matrix form and each consisting of a first MISFET and an information storing capacitor both connected in series with each other, and also having a peripheral circuitry constituted by a plurality of second MISFETs, said method comprising:

(a) a step of forming a first gate electrode of each said first MISFET and a second gate electrode of each said second MISFET over first and second regions, respectively, of a first electroconductivity type **semiconductor** substrate;

(b) a step of introducing first impurities of a second electroconductivity type, opposite to the first electroconductivity type, into said **semiconductor** substrate in self-alignment with said first and second gate electrodes, so as to form first **semiconductor** regions for the first and second MISFETs;

(c) a step of forming a side wall **insulating film** along end portions of said first and second gate electrodes;

(d) a step of forming a first electrode of said information storing capacitor so as to be in contact with one of the source and drain regions of said first MISFET;

(e) a step of forming a **dielectric film** and a second electrode of said information storing capacitor on said first electrode;

(f) a step of forming a **second insulating film** over said first and second regions of said **semiconductor** substrate, overlying the second gate electrode over the second region and overlying the second electrode over the first region;

(g) a step of forming a wiring **layer** over said **second insulating film** in said first and second regions;

(h) a step of introducing second impurities of said second electroconductivity type into said **semiconductor** substrate over

said second region in self-alignment with said second gate electrode and said side wall **insulating film**, so as to form second **semiconductor** regions for said second MISFETs, after having carried out processes (a) and (c); and

(i) a step of forming a third **insulating film** overlying only said second region,

wherein said process (h) is carried out prior to said processes (i) and (f), and said process (i) is carried out between said processes (c) and (g).

Dwg.1/20

US 5389558 A

The method for fabricating a **semiconductor** memory **circuit** device having a **matrix** array of memory cells, each contg. a first MISFET and an information storing capacitor connected in series, and peripheral circuitry including second MISFETs. The method comprises forming a first gate electrode of each first MISFET and a second gate electrode of each second MISFET in two regions, respectively, on a **semiconductor** substrate. First N-type impurities are introduced into the substrate in self-alignment **w** .r.t. the two gate electrodes to form source and drain regions for the two MISFETs. A third **insulating film** is formed in both regions on the substrate, and is partially removed to expose one of the source and drain regions of the first MISFET.

A first electrode of the capacitor is formed in contact with the exposed source or drain region of the first MISFET. A **dielectric film** and a second capacitor electrode are formed in sequence on the first electrode, and a **second insulating film** is formed on the third **insulating film** in the two regions of the substrate. A wiring layer is formed on the **second insulating film** in the two regions, and the two electrodes extend on the third **insulating film** in the first region. The thickness of the third **insulating film** is larger than a total thickness of the two capacitor electrodes.

USE/ADVANTAGE - E.g. for microcomputer circuit incorporating DRAM or SRAM. Improved integration density and product yield during mfr.

Dwg.1/20

54/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7163108 INSPEC Abstract Number: B2002-03-2560R-003
Title: Polycrystalline silicon **thin-film transistors**
Author(s): Wagner, S.; Wu, M.; Min, B.-G.R.; Cheng, I.-C.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Journal: Diffusion and Defect Data Part B (Solid State Phenomena)
Conference Title: Diffus. Defect Data B, Solid State Phenom. (Switzerland)
vol.80-81 p.325-36
Publisher: Balaban Publishers; Scitec Publications,
Publication Date: 2001 Country of Publication: Switzerland
CODEN: DDBPE8 ISSN: 1012-0394
SICI: 1012-0394(2001)80/81L.325:PSTF;1-D
Material Identity Number: B404-2001-002
Conference Title: Polycrystalline Semiconductors VI. Materials, Technologies, and Large Area Electronics. Sixth International Conference
Conference Sponsor: Centre National de la Recherche Sci.; Region Bretagne ; Conseil General d'Ille et Vilaine; et al
Conference Date: 3-7 Sept. 2000 Conference Location: St. Malo, France
Language: English
Abstract: Silicon **thin film transistors** (TFTs) with high performance are important components of flexible large area electronics. We discuss two Si **TFT** technologies fabricated at the opposite ends of the range of process temperatures. Nanocrystalline silicon (nc-Si:H) TFTs are made at 250 degrees C and achieve **n channel** operation with an electron mobility up to 40 cm/sup 2/V/sup -1/s/sup -1/, and also p channel operation. These n and p channel TFTs can be integrated to complementary CMOS circuits, and thus are candidates for integrating active **matrix** and **driver circuits** in a low temperature silicon technology. Microcrystalline silicon (mu c-Si) on passivated steel foils lies at the high end of process temperature, which may reach 950 degrees C. We have evolved three generations of device processes for mu c-Si TFTs. They go from an all deposited non self-aligned structure over a self-aligned ion-implanted configuration to the incorporation of a thermal oxide gate insulator. These two new polycrystalline silicon **TFT** technologies reflect the ability of silicon to adapt to plastic and metal substrates. Their perfection will pose considerable demands on silicon film growth, device processing, and on theoretical understanding.
Subfile: B

54/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02794422
E.I. Monthly No: EIM8909-032779
Title: Very small active-matrix LCD panel with monolithically integrated peripheral **driver circuits**.
Author: Emoto, F.; Senda, K.; Fujii, E.; Nakamura, A.; Yamamoto, A.; Uemoto, Y.; Kamimura, T.; Kano, G.
Corporate Source: Matsushita Electric Corp, Takatsuki, Jpn
Conference Title: Technical Digest - International Electron Devices Meeting 1988
Conference Location: San Francisco, CA, USA Conference Date: 19881211
E.I. Conference No.: 12244
Source: Tech Dig Int Electron Devices Meet 1988 Technical Digest - International Electron Devices Meeting. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 88CH2528-8), Piscataway, NJ, USA. p 878-880
Publication Year: 1988
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: The authors demonstrate a very small active-matrix LCD (liquid crystal display) panel, 21 mm multiplied by 25 mm, having **driver circuits** on a single quartz substrate. In order to increase the channel mobility of the **TFT**, a novel technology for solid-phase growth of the polysilicon film on the quartz substrate was developed. The typical subthreshold characteristics of the fabricated p- and **n-channel** TFTs in the polysilicon film are reported. An LCD panel containing the peripheral **driver circuits** and the active **matrix** has been successfully fabricated by the conventional CMOS process. The output signal waveforms of the fabricated horizontal shift register are shown. 3 Refs.

54/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013936792
WPI Acc No: 2001-421006/200145
XRAM Acc No: C01-127680
XRPX Acc No: N01-311922
Thin film transistor for **drive circuit** of integrated active **matrix** liquid crystal display device, has fixed electric charge on side wall of gate electrode, based on which transistor is judged to be p-channel or **n-channel**
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001111055	A	20010420	JP 99284362	A	19991005	200145	B

Priority Applications (No Type Date): JP 99284362 A 19991005
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001111055	A		5	H01L-029/786	

Abstract (Basic): JP 2001111055 A
Abstract (Basic):
NOVELTY - A **semiconductor** thin film is formed on a substrate (1) above which a gate insulating film (4) is formed. A gate electrode (5) is formed above the gate insulating film if the fixed charge on the side wall of gate electrode is negative then the transistor is judged to be **n-channel** else the transistor is judged to be p-channel.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **thin film transistor** manufacturing method.
USE - For switching element and **drive circuit** of integrated active **matrix** liquid crystal display device.
ADVANTAGE - Efficient LDD area is formed without impurity injection and thereby damage of LDD area is prevented. The hydrogenation process of polycrystalline Si film is reduced, due to the formation of insulating film.
DESCRIPTION OF DRAWING(S) - The figure shows the production process of **thin film transistor**. (Drawing includes non-English language text).
Substrate (1)
Gate insulating film (4)
Gate electrode (5)
pp; 5 DwgNo 1/4

54/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013819343
WPI Acc No: 2001-303555/200132
XRPX Acc No: N01-218096
Semiconductor device e.g. electro-optical apparatus used in electronic device, includes n-type impurity in LDD area of **drive circuit**, whose concentration is higher than that of LDD area of pixel circuit
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME); SHARP KK (SHAF)
Inventor: KASAHARA K; KAWASAKI R; KITAKADO H; OGAWA H; TOMIYASU K; YAMAZAKI S
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001007343	A	20010112	JP 2000118683	A	20000419	200132	B
KR 2001014785	A	20010226	KR 200020950	A	20000420	200156	
US 6362507	B1	20020326	US 2000550828	A	20000418	200226	
TW 459272	A	20011011	TW 2000107398	A	20000419	200247	

Priority Applications (No Type Date): JP 99111592 A 19990420
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001007343	A		25	H01L-029/786	
KR 2001014785	A			H01L-029/786	
US 6362507	B1			H01L-027/03	
TW 459272	A			H01L-021/00	

Abstract (Basic): JP 2001007343 A
Abstract (Basic):
NOVELTY - A gate insulating film is formed between activated layers with **pixel matrix** and **drive circuits**, and substrate. The **n-channel** type TFTs have gate electrodes (202-204) provided between insulating film and substrate, so that gate electrodes of TFTs overlap with LDD area of pixel and **drive circuits**, respectively. Concentration of n-type impurity in LDD area of **drive circuit** is more than that of pixel circuit.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor device** production procedure.
USE - E.g. electro-optical apparatus used as active matrix type liquid crystal display device, mounted in electronic device.
ADVANTAGE - Enables to configure **TFT** of suitable capability depending on the specification, hence operating characteristic and reliability are raised greatly.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of pixel and **drive circuits**.
Gate electrodes (202-204)
pp; 25 DwgNo 2/24

54/3,AB/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013633080
WPI Acc No: 2001-117288/200113
XRPX Acc No: N01-086749

Semiconductor device for active matrix liquid crystal display, has TFTs in **drive** and **pixel matrix circuits**, in which area of LDD overlapping and not overlapping gate electrode are formed respectively

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: KASAHARA K; KAWASAKI R; KITAKADO H; YAMAZAKI S

Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000340801	A	20001208	JP 200081378	A	20000323	200113 B
US 6281552	B1	20010828	US 2000532690	A	20000322	200151
US 20010045558	A1	20011129	US 2000532690	A	20000322	200202
			US 2001905587	A	20010713	

Priority Applications (No Type Date): JP 9978715 A 19990323
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000340801	A		20	H01L-029/786	
US 6281552	B1			H01L-029/04	
US 20010045558	A1			H01L-029/76	Cont of application US 2000532690 Cont of patent US 6281552

Abstract (Basic): JP 2000340801 A
Abstract (Basic):

NOVELTY - The **semiconductor device** has **drive circuit** and **pixel matrix circuit**. Lightly doped drain (LDD) area of the **N-channel thin film transistor** (**TFT**) of the **drive circuit** is formed so that it overlaps with gate electrode of that **TFT**. LDD area of **N-channel TFT** of **pixel matrix circuit** is formed so that it does not overlap with gate electrode of that **TFT**.

DETAILED DESCRIPTION - The n-type impurity concentration of the LDD area of the **N-channel TFT** of the **drive circuit** is higher than that of LDD area of **N-channel TFT** of the **pixel matrix circuit**. An INDEPENDENT CLAIM is also included for **semiconductor device** manufacturing method.

USE - **Semiconductor device** for active matrix liquid crystal display, electroluminescence display used in projector and other electronic devices.

ADVANTAGE - Operating characteristics and reliability of the **semiconductor device** are improved by using **TFT** of suitable capability and specification. Reduces OFF current value and reduces degradation of ON state current by reducing impurity concentration of LDD area of **TFT** of **pixel matrix**

circuit and by increasing impurity concentration of LDD area of **TFT** of **drive circuit**, hence reduces power consumption of pixel **circuit** and increases current **drive** capability.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view explaining the **pixel matrix circuit** and **drive circuit** manufacturing processes involved.

pp; 20 DwgNo 1/18

54/3,AB/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010584124
WPI Acc No: 1996-081077/199609
Related WPI Acc No: 2002-036228
XRAM Acc No: C96-026592
XRPX Acc No: N96-067466

Semiconductor IC for **drive circuit** e.g. active **matrix circuit**, LCD - has triangle shaped sidewalls on both sides of gate electrode and gate wiring

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7321337	A	19951208	JP 94137987	A	19940526	199609	B

Priority Applications (No Type Date): JP 94137987 A 19940526
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7321337	A		16	H01L-029/786	

Abstract (Basic): JP 7321337 A

The **semiconductor** IC has an **N-channel** type **thin film transistor**. The anodic film is formed by performing the anodic oxidation of material which constitutes the gate electrode and gate wiring. An insulation film (110) is formed adjoining a silicon nitride film (108), which covers the entire active region. The insulation film is etched to leave triangular shaped sidewalls adjoining gate structure.

USE/ADVANTAGE - In image sensor, microprocessor, **semiconductor** memory. Prevents breakage of second layer wiring

54/3,AB/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010320536
WPI Acc No: 1995-221808/199529
Related WPI Acc No: 1995-221804; 1998-227031; 2002-245781
XRPX Acc No: N95-173878
Thin film **semiconductor** integrated circuit e.g. MOSFET for display **drive circuit** or SRAM - has peripheral **drive circuits** formed along with active **matrix circuit** made from **thin film transistors** in same package
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME); TAKEMURA Y (TAKE-I); YAMAGUCHI N (YAMA-I); ZHANG H (ZHAN-I)
Inventor: TAKEMURA Y; YAMAGUCHI N; ZHANG H
Number of Countries: 004 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7135324	A	19950523	JP 93301174	A	19931105	199529	B
US 5648277	A	19970715	US 94334335	A	19941102	199734	
CN 1111815	A	19951115	CN 94119925	A	19941105	199737	
US 6218678	B1	20010417	US 94334335	A	19941102	200123	
			US 97815070	A	19970311		
US 20010007357	A1	20010712	US 94334335	A	19941102	200143	
			US 97815070	A	19970311		
			US 2001769374	A	20010126		
US 20010014496	A1	20010816	US 94344335	A	19941122	200149	
			US 97815070	A	19970311		
			US 2001779826	A	20010209		
KR 294088	B	20010917	KR 9428842	A	19941104	200231	

Priority Applications (No Type Date): JP 93301174 A 19931105; JP 93301176 A 19931105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7135324	A		9	H01L-029/786	
US 5648277	A		17	H01L-021/336	
CN 1111815	A			H01L-021/00	
US 6218678	B1			H01L-029/04	Div. ex application US 94334335 Div ex patent US 5648277
US 20010007357	A1			H01L-021/425	Div ex application US 94334335 Div ex application US 97815070 Div ex patent US 5648277 Div ex patent US 6218678
US 20010014496	A1			H01L-021/336	Div ex application US 94344335 Div ex application US 97815070 Div ex patent US 5685302 Div ex patent US 6218678
KR 294088	B			H01L-029/78	Previous Publ. patent KR 95015820

Abstract (Basic): JP 7135324 A
The device has its P type (121) and N type (123) low-concentration impurity domains holding their respective impurity domains (120,122)

formed on the ground insulating film (102) laid above the substrate (101). A titanium metal film (124) laid above them forms the silicide domains (125-127).

The inter-layer insulating material (128) is then placed over them and an amorphous silicon (129) is added on one side. The device is equipped with metal wires (133-136) made from nitride titanium alloy that connect to the silicide domains and the N type micro-crystal silicon (130,131). The N type impurity domain, P type impurity domain, and the amorphous silicon form the **N channel** peripheral **drive circuit** (137), the P channel peripheral **drive circuit** (138), and the active **matrix circuit** (139), respectively.

ADVANTAGE - Provides optimised performance from single package.

Dwg.2/4

Abstract (Equivalent): US 5648277 A

A method of mfg. a **semiconductor device** comprising the steps of:

forming a **semiconductor** layer on an insulating surface;

forming a first insulating film on the **semiconductor** layer;

forming a gate electrode on the first insulating film;

forming a first anodic oxide film on side surfaces of the gate electrode by applying an electric current to the gate electrode in an electrolyte;

etching the first insulating film in order to thin or remove the insulating film using the first anodic oxide film as a mask, thereby forming a gate insulating film;

removing the first anodic oxide film after the etching; and

introducing ions of an impurity of an N or P type conductivity into a portion of the **semiconductor** layer using the gate electrode and the gate insulating film as a mask,

where the introducing is carried out with at least two different conditions having a higher acceleration voltage and a lower acceleration voltage.

A method of mfg. a **semiconductor device** comprising the steps of:

forming a **semiconductor** layer on an insulating surface;

forming an insulating film on an entire surface of the **semiconductor** layer;

forming a gate electrode on the insulating film;

patterning the insulating film into a gate insulating film in such a manner that the gate insulating film extends beyond side edges of the gate electrode but does not completely cover the **semiconductor** layer so that portions of the **semiconductor** layer are exposed; and

introducing one conductivity type impurity ions into the **semiconductor** layer using the gate electrode and the gate insulating layer as a mask,

where a condition of the introducing step is selected so that regions of the **semiconductor** layer located below extensions of the gate insulating film beyond the gate electrode are added with the impurity at a first concentration while exposed regions of the **semiconductor** layer are added with the impurity at a second concentration which is different from the first concentration,

where the insulating film is patterned by using a mask which is an

anodic oxide film formed on side surfaces of the gate electrode

54/3,AB/8 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06779867
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2001-007343 [JP 2001007343 A]
PUBLISHED: January 12, 2001 (20010112)
INVENTOR(s): OGAWA HIROYUKI
TOMIYASU KAZUHIDE
KAWASAKI RITSUKO
KITAKADO HIDETO
KASAHARA KENJI
YAMAZAKI SHUNPEI
APPLICANT(s): SHARP CORP
SEMICONDUCTOR ENERGY LAB CO LTD
APPL. NO.: 2000-118683 [JP 2000118683]
FILED: April 19, 2000 (20000419)
PRIORITY: 11-111592 [JP 99111592], JP (Japan), April 20, 1999 (19990420)

ABSTRACT

PROBLEM TO BE SOLVED: To enhance the performance characteristic and the reliability of a **semiconductor device**, by a method wherein the structure of a **thin-film transistor TFT** which is arranged on every circuit of the **semiconductor device** is made proper according to the function of the **circuit**.

SOLUTION: An active **matrix** substrate which comprises a **pixel** part and its **drive circuit** is formed on the same substrate. An **n-channel TFT** 141 and a p-channel **TFT** 140 are formed in the **drive circuit**. An **n-channel TFT** 142 is formed in the pixel part. In addition, a capacitance interconnection 106 which is formed simultaneously with a gate electrode, an insulating film which is formed of the same material as a gate insulating film, and a **semiconductor** layer 145 which is connected to the source or drain region 125 of the **n-channel TFT** 142 and with which an impurity element used to give an n-type is doped, constitute a holding capacitance 143. Consequently, the structure of every **TFT** constituting every circuit is optimized according to specifications required by the pixel part and the **drive circuit** and the operating performance and the reliability of this **semiconductor device** can be enhanced.

54/3,AB/9 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06713634

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-299469 [JP 2000299469 A]
PUBLISHED: October 24, 2000 (20001024)
INVENTOR(s): YAMAZAKI SHUNPEI
MURAKAMI TOMOHITO
KOYAMA JUN
TANAKA YUKIO
KITAKADO HIDETO
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD
APPL. NO.: 2000-033377 [JP 200033377]
FILED: February 10, 2000 (20000210)
PRIORITY: 11-033623 [JP 9933623], JP (Japan), February 12, 1999 (19990212)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the opening ratio of the **pixel** section of an active-**matrix** liquid crystal display device in which **drive circuits** such as a shift register, a buffer circuit, etc., are mounted on the same substrate, and at the same time, to provide an optimum **TFT** constitution.

SOLUTION: In a buffer circuit, an **n-channel TFT** provided with an LDD overlapping a gate electrode is formed, and in the **n-channel TFT** of a pixel section, an LDD which does not overlap the gate electrode is provided. The retention volume provided in the pixel section is formed of a light shielding film 156, a dielectric film 157 formed on the film 156, and pixel electrodes 160. In particular, the light shielding film 156 is constituted of an aluminum film, and the dielectric film 157 is constituted of an aluminum oxide film formed by anodic oxidation.

54/3,AB/10 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06180211

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-121760 [JP 11121760 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): YAMAZAKI SHUNPEI
OTANI HISASHI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD
APPL. NO.: 09-303527 [JP 97303527]
FILED: October 17, 1997 (19971017)

ABSTRACT

PROBLEM TO BE SOLVED: To form a **thin film transistor** on a substrate which can be enlarged in area at a low cost, by a method wherein an insulating silicon film is formed on the both sides of a glass substrate where a distortion point is specified.

SOLUTION: An amorphous silicon film 102 is formed on the surface, rear, and side of a substrate 101 whose distortion temperature is 750°C or above through a low pressure thermal CVD method so as to wrap up the substrate 101. Then, the substrate 101 is thermally treated to turn the amorphous silicon film 102 into a thermal oxide film 103 by thermal oxidation. Then, an amorphous silicon film 104 is formed through the low pressure thermal CVD method and a plasma CVD method, cleaned, and then turned into a high-temperature polysilicon film 105 by furnace annealing. Then, a **drive circuit** formed of a CMOS circuit where an NTFT(**N-channel TFT**) and a P-channel **TFT** are complementarily combined and a **pixel matrix circuit** formed of NTFTs are integrally formed on the same substrate.

54/3,AB/11 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05861829

ACTIVE MATRIX TYPE DISPLAY UNIT AND ITS MANUFACTURING METHOD

PUB. NO.: 10-144929 [JP 10144929 A]
PUBLISHED: May 29, 1998 (19980529)
INVENTOR(s): SHIBUYA TSUKASA
YOSHINOUCHI ATSUSHI
CHIYOU KOUYUU
TAKEUCHI AKIRA
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-315486 [JP 96315486]
FILED: November 12, 1996 (19961112)

ABSTRACT

PROBLEM TO BE SOLVED: To selectively arrange **thin-film transistors** provided with necessary characteristics in a **pixel matrix** part and a peripheral **drive circuit** part of an active matrix type display device.

SOLUTION: In an arrangement provided with a **pixel matrix** part and a peripheral device circuit part on the same substrate, in both **N-channel** driver parts of the **pixel matrix** part and peripheral **drive circuit** part, there are formed **N-channel** type **thin-film transistors** provided with source and drain regions 108, 110, 111, 113 formed in a nonself-aligning process. Further low concentration impurity regions 127, 130, 131, 133 are formed in a self-aligning process. Further, in a P-channel driver part of the peripheral **drive circuit** part, there are formed P-channel type **thin-film transistors** which form source and drain regions 134, 136 by only the self-aligning process, without forming the low-concentration impurity region.

54/3,AB/12 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05692317
ACTIVE-**MATRIX CIRCUIT**

PUB. NO.: 09-307117 [JP 9307117 A]
PUBLISHED: November 28, 1997 (19971128)
INVENTOR(s): YAMAZAKI SHUNPEI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-140790 [JP 96140790]
FILED: May 10, 1996 (19960510)

ABSTRACT

PROBLEM TO BE SOLVED: To make it possible to form a monolithic active-**matrix circuit** reconciled with the high-speed operation of a **driver circuit** by a method wherein lightly doped regions are provided in an **N-channel** transistor and are not provided in a P-channel transistor and a crystalline silicon film is utilized for the **driver circuit**.

SOLUTION: Phosphrous is implanted in an active layer 12a of an **N-channel TFT** using a mask 15c covering active layers 12b and 12c of a P-channel **TFT** and a mask 15b covering a prescribed part of the layer 12a to form a source 16a and a drain 16a of the **N-channel TFT** . As phosphorus is not implanted in the region, which is covered with the mask 15b, of the weak N-type region of the layer 12a of the **N-channel TFT** in the following doping, the region, which is covered with the mask 15b, remains as the weak N-type region, whereby lightly doped regions 17 are formed. After that, a thermal annealing is performed, damage due to the doping is made to activate and the crystallinity of silicon is made to recover. After that, a silicon oxide film 18 is formed.

54/3,AB/13 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04249431
LIQUID CRYSTAL DISPLAY DEVICE

PUB. NO.: 05-241131 [JP 5241131 A]
PUBLISHED: September 21, 1993 (19930921)
INVENTOR(s): INO MASUMITSU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-080453 [JP 9280453]
FILED: March 02, 1992 (19920302)
JOURNAL: Section: P, Section No. 1666, Vol. 17, No. 703, Pg. 56, December 22, 1993 (19931222)

ABSTRACT

PURPOSE: To prevent the temperature rise by the generation of heat in the active matrix type liquid crystal display device.

CONSTITUTION: An active matrix substrate 1 and a counter substrate 2 are disposed to face each other via a prescribed spacing and a liquid crystal layer 3 is held in this spacing. A horizontal **driving circuit** part and a vertical **driving circuit** part are also formed in addition to a display part on the active matrix substrate 1 to constitute a monolithic structure. The display part includes picture element **electrodes** arranged in a **matrix** form and **thin-film transistors** (TFTs) **driving** these picture element **electrodes**. On the other hand, the **driving circuit** parts are constituted of the TFTs integrated at a high density and include, for example, **N channel** TRs4 P channel TRs 5, etc. The heat is generated by the operation of these TRs 4, 5. A heat conduction member 17 facing the heat generating region is provided on the side of the active matrix substrate 1 opposite from the side in contact with the liquid crystal layer. This heat conduction member 17 is brought into pressurized contact with the above- mentioned region by a supporting member 18.

57/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014536057
WPI Acc No: 2002-356760/200239
Related WPI Acc No: 1996-126309; 2001-527087; 2002-201091; 2002-201092; 2002-248785
XRPX Acc No: N02-280523
Insulated gate type **thin-film transistor** has **first** gate **wiring** that crosses layer insulation object via first insulating film and source wiring formed on layer insulation object on second gate electrode
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002057345	A	20020222	JP 94180950	A	19940707	200239	B
			JP 2001143559	A	19940707		

Priority Applications (No Type Date): JP 94180950 A 19940707; JP 2001143559 A 19940707
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002057345	A		15	H01L-029/786	Div ex application JP 94180950

Abstract (Basic): JP 2002057345 A
Abstract (Basic):

NOVELTY - The **TFT** has a **first** gate **wiring** that crosses an layer insulation object through a first insulating film. A source wiring is formed on the layer insulation object on a second gate electrode which is electrically connected to the **first** gate **wiring** for every pixel. The first gate electrode is extended from the **first** gate **wiring**.

DETAILED DESCRIPTION - The second gate electrode is formed on the second insulating film on a crystalline **semiconductor** layer. The crystalline **semiconductor** layer is formed on the first insulating film formed on the first gate electrode. A pixel electrode is connected to the **TFT** which is included in each **pixel** of an active **matrix circuit**. A data **driver circuit** and a scan **drive circuit** are provided for the **TFT**.

USE - For e.g. active matrix type liquid-crystal display device, image sensor.

ADVANTAGE - Offers insulated gate type **TFT** with favorable display property. Uses reduced number of resistors in gate wiring double layer structure of gate wiring, thus reducing disconnection defect of gate wiring. Ensures reduced parasitic capacitance in crossed section of gate wiring and source wiring.

DESCRIPTION OF DRAWING(S) - The figure shows the structure of insulated gate type **TFT**

57/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014470652
WPI Acc No: 2002-291355/200233
XRAM Acc No: C02-085438
XRPX Acc No: N02-227490
Active matrix liquid crystal display device has display area having set of pixel regions with respective first **thin film transistors**, and **driving-circuit**-forming area having second **thin film transistors**
Patent Assignee: HITACHI MFR CO LTD (HITA); HITACHI LTD (HITA)
Inventor: HASEGAWA A
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020021380	A1	20020221	US 2001919916	A	20010802	200233	B
JP 2002131783	A	20020509	JP 2001218144	A	20010718	200234	
CN 1337590	A	20020227	CN 2001125207	A	20010809	200234	

Priority Applications (No Type Date): JP 2000241472 A 20000809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020021380	A1		12	G02F-001/1343	
JP 2002131783	A		9	G02F-001/1368	
CN 1337590	A			G02F-001/136	

Abstract (Basic): US 20020021380 A1
Abstract (Basic):

NOVELTY - An active matrix liquid crystal display device has display area having a set of pixel regions with respective first **thin-film transistors** (**TFT**). A **driving-circuit**-forming area having second TFTs is located outside the display area. A gate electrode of first **TFT** is made of a material different than gate signal line. A gate electrode of second **TFT** is made of a material different than wiring layer.

DETAILED DESCRIPTION - An active matrix liquid crystal display device consists of a display area and a **driving-circuit**-forming area outside the display area.

The display area includes a set of pixel regions, each having a first **thin-film transistor** (**TFT**).

The **driving-circuit**-forming area has second TFTs.

The gate electrode of first **TFT** is made of a material that is different than a gate signal line (GL). The gate electrode of first **TFT** is electrically connected to the gate signal line.

The gate electrode of each second **TFT** is made of a material that is different than a wiring layer or electrode. The gate electrode of second **TFT** is electrically connected to the wiring layer or electrode.

The gate electrodes (GT) of first and second TFTs are made of the same material.

The gate signal **line** and the **wiring** layer or electrode

are made of the same material.

USE - As active matrix liquid crystal display device.

ADVANTAGE - Integration densities of gate-signal-line **driving circuit** and drain-signal-line **driving circuit** are increased.

DESCRIPTION OF DRAWING(S) - The figure is a plan view showing the structure of each **pixel** of the inventive active **matrix** display device.

Semiconductor layer (AS)
Drain signal line (DL)
Gate signal line (GL)
Gate electrodes (GT)
Pixel electrode (PIX)

57/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013217318
WPI Acc No: 2000-389192/200034
XRPX Acc No: N00-291439
Semiconductor device with **thin film transistors**, e.g. liquid crystal display or other electro-optical display device; has **thin film transistor** formed on substrate with gate electrode on gate insulating film contacting **semiconductor** layer
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: YAMAZAKI S
Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1005094	A2	20000531	EP 99123427	A	19991124	200034	B
JP 2000223716	A	20000811	JP 99334453	A	19991125	200044	

Priority Applications (No Type Date): JP 98333623 A 19981125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1005094	A2	E	60	H01L-029/786	
JP 2000223716	A		35	H01L-029/786	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 1005094 A2
Abstract (Basic):
NOVELTY - The device has at least one **thin film transistor** formed over a substrate (101), which a gate insulating film (103) contacting a **semiconductor** layer, with a gate electrode contacting the gate insulating film.
DETAILED DESCRIPTION - The gate electrode has a first layer (113,116) contacting the gate insulating film, a second layer (114,117) formed on and inside the edge of the top face of the first layer, and a third layer (115,118) contacting the first two layers. The **semiconductor** layer has a channel forming region (104,109), a first impurity region (107,108) of one conductivity type and a second impurity region (105,106a,106b) of the same conductivity type formed between the channel forming region and the first impurity region. Part of the second impurity region lies under the first layer of the gate electrode.
An INDEPENDENT CLAIM is included for a method for fabricating the device.
USE - E.g. liquid crystal display or other electro-optical display device.
ADVANTAGE - Suitable for liquid crystal display device of active **matrix** type in which a pixel **matrix circuit** and **driver circuits** require different **drive** voltages and different **thin film transistor** characteristics.
DESCRIPTION OF DRAWING(S) - The figure shows a cross section of

thin film transistors in the device.
substrate (101)
underlying film (102)
gate insulating film (103)
channel forming regions (104,109)
second impurity regions (105,106a,106b)
first impurity regions (107,108)
third impurity of p-channel **thin film transistor** (111,112)
first layers of gate electrodes (113,116)
second layers of gate electrodes (114,117)
third layers of gate electrodes (115,118)
first interlayer insulating film (119)
source **wiring lines** (120,121)
drain **wiring line** (122)
passivation film (123)
second interlayer insulating film (124)

57/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05710569

ACTIVE **MATRIX** PANEL AND **DRIVING CIRCUIT** FOR THE SAME

PUB. NO.: 09-325369 [JP 9325369 A]
PUBLISHED: December 16, 1997 (19971216)
INVENTOR(s): MISAWA TOSHIYUKI
OSHIMA HIROYUKI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-025683 [JP 9725683]
FILED: February 07, 1997 (19970207)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain an active matrix panel which is of optically fine and is of compact and is excellent in reliability by alternately arranging plural first wirings and plural second wirings and alternately arranging first silicon thin films and second silicon thin films in between adjacent **first wiring** and **second wiring**.

SOLUTION: Unit cells of a **driver circuit** are formed in areas 196-198 surrounded by a broken **line** which includes a **wiring** for positive power source 184, a wiring for negative power source 185, silicone thin films 186-191 of P type TFTs and silicone thin films 192-195 of N type TFTs. Since the separating of elements of respective TFTs is performed by etching silicone thin films in island shapes, for example, the distance (a) between the island 192 of the silicon thin film for the N type **TFT** and the island 187 of the silicon thin film for the P type **TFT** and the distance (b) between two islands 187, 188 of the silicone thin films for the P type TFTs can be made almost equal. Thus, the degree of integration of a direction along which the unit cells is repeated is enhanced by alternately arranging islands of the P type TFTs and islands of the N type TFTs.

61/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014425077
WPI Acc No: 2002-245780/200230
Related WPI Acc No: 1994-141747; 1995-010505; 1998-199210; 1999-391305; 1999-391378; 2000-249437; 2000-288761; 2001-097137; 2001-427862; 2002-077580; 2002-245779; 2002-260689
XRAM Acc No: C02-073795
XRPX Acc No: N02-190560

Insulated gate type **semiconductor device** for **thin film transistor** used in liquid crystal display device, has metallic wirings and electrodes that are formed on gate **insulating film**

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001185735	A	20010706	JP 98262315	A	19931020	200230	B
			JP 2000322036	A	19931020		

Priority Applications (No Type Date): JP 9345786 A 19930210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001185735	A		22	H01L-029/786	Div ex application JP 98262315

Abstract (Basic): JP 2001185735 A
Abstract (Basic):

NOVELTY - Aluminum nitride film (102) and **silicon oxide** film (103) are formed on both sides of a substrate (101). A crystalline film (104) and the gate **insulating film** (105) are formed on the **silicon oxide** film. The metallic wirings (112, 113) and the electrodes (111) are formed on gate **insulating film**.

DETAILED DESCRIPTION - The aluminum nitride film includes boron, silicon, carbon and oxygen.

USE - For **drive circuit** of active **matrix** liquid crystal display (LCD) device, image sensor, silicon on insulator (SOI), integrated circuit (IC), microprocessor, microcontroller, microcomputer, **semiconductor** memory, etc.

ADVANTAGE - Reduces size of **thin film transistor** (**TFT**) by enabling proper arrangement of active layer and contact. Enables effective usage of large area substrate for **TFT** formation.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of **TFT** manufacturing process.

Substrate (101)
Aluminum nitride film (102)
Silicon oxide film (103)
Crystalline film (104)
Gate **insulating film** (105)
Electrode (111)
Metallic wirings (112, 113)
pp; 22 DwgNo 1/6

61/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013087364
WPI Acc No: 2000-259236/200023
XRAM Acc No: C00-079463
XRPX Acc No: N00-192864
Apparatus having integrated circuits made of **thin film transistor** devices has **second insulating film** and **semiconductor film** formed successively without exposure to the atmosphere
Patent Assignee: SEL SEMICONDUCTOR ENERGY LAB (SEME); SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: KASAHARA K
Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 993032	A2	20000412	EP 99119516	A	19991001	200023	B
JP 2000183360	A	20000630	JP 99274106	A	19990928	200037	

Priority Applications (No Type Date): JP 98283711 A 19981006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 993032	A2	E	30	H01L-021/331	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2000183360	A		26	H01L-029/786	

Abstract (Basic): EP 993032 A2
Abstract (Basic):
NOVELTY - Device includes **first insulating layer** on a substrate and heat-treated, **second insulating film** on the **first insulating film**, and semiconductor **film** on the **second insulating film**. The **second insulating** and semiconductor **films** are formed successively without exposure to the atmosphere. Hence the interface between an active layer, particularly a channel forming region, and a base film is improved.
DETAILED DESCRIPTION - The **semiconductor device** includes:
(a) a 100-500 nm thick **first insulating film** formed over a substrate;
(b) a 10-100 **second insulating film** in contact with the **first insulating film**;
(c) a channel-forming region and source and drain regions formed on both sides of the channel forming region which is formed in contact with the **second insulating film**;
(d) a gate **insulating layer** in contact with the channel forming region; and
(e) a gate line provided over the channel forming region with the gate **insulating layer** interposed between them.
The impurity concentration in the layer at the interface between the first and **second insulating films** is higher than

that in an interface between the **second insulating film** and the channel forming region.

A low concentration impurity region is formed between the channel; forming region and the source region or between the channel forming region and the drain region.

The **second insulating film** and the channel forming region are formed by successive formation in laminated layers without exposure to the atmosphere.

A catalytic element that accelerates crystallization of silicon is contained in at least the source region and the drain regions.

INDEPENDENT CLAIMS are given for methods of manufacturing a **semiconductor device**, where the **first insulating film** is heat-treated at 200-700 degrees C.

USE - For **semiconductor** apparatus such as **thin film transistors** (**TFT**) and MOS transistors, and also displays and electrooptic apparatus, such as image sensors.

ADVANTAGE - Improved interface between an active layer, particularly a channel forming layer, and a base film to improve ,e.g., **TFT** characteristics. High reliability of **semiconductor device**.

DESCRIPTION OF DRAWING(S) - The device shows the construction of a **semiconductor** apparatus (liquid crystal display).

Glass substrate (500)
Pixel matrix circuit (501)
Scan line **drive circuit** (502)
Signal line **drive circuit** (503)
Flexible printed circuit (510)
IC chip (511, 512)
Logic circuit (520)
Counter substrate (530)

61/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013087364
WPI Acc No: 2000-259236/200023
XRAM Acc No: C00-079463
XRPX Acc No: N00-192864
Apparatus having integrated circuits made of **thin film transistor** devices has **second insulating film** and **semiconductor film** formed successively without exposure to the atmosphere
Patent Assignee: SEL SEMICONDUCTOR ENERGY LAB (SEME); SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: KASAHARA K
Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 993032	A2	20000412	EP 99119516	A	19991001	200023	B
JP 2000183360	A	20000630	JP 99274106	A	19990928	200037	

Priority Applications (No Type Date): JP 98283711 A 19981006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 993032	A2	E	30	H01L-021/331	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000183360	A		26	H01L-029/786	

Abstract (Basic): EP 993032 A2
Abstract (Basic):
NOVELTY - Device includes **first insulating layer** on a substrate and heat-treated, **second insulating film** on the **first insulating film**, and semiconductor **film** on the **second insulating film**. The **second insulating** and semiconductor **films** are formed successively without exposure to the atmosphere. Hence the interface between an active layer, particularly a channel forming region, and a base film is improved.
DETAILED DESCRIPTION - The **semiconductor device** includes:
(a) a 100-500 nm thick **first insulating film** formed over a substrate;
(b) a 10-100 **second insulating film** in contact with the **first insulating film**;
(c) a channel-forming region and source and drain regions formed on both sides of the channel forming region which is formed in contact with the **second insulating film**;
(d) a gate **insulating layer** in contact with the channel forming region; and
(e) a gate line provided over the channel forming region with the gate **insulating layer** interposed between them.
The impurity concentration in the layer at the interface between the first and **second insulating films** is higher than

that in an interface between the **second insulating film** and the channel forming region.

A low concentration impurity region is formed between the channel; forming region and the source region or between the channel forming region and the drain region.

The **second insulating film** and the channel forming region are formed by successive formation in laminated layers without exposure to the atmosphere.

A catalytic element that accelerates crystallization of silicon is contained in at least the source region and the drain regions.

INDEPENDENT CLAIMS are given for methods of manufacturing a **semiconductor device**, where the **first insulating film** is heat-treated at 200-700 degrees C.

USE - For **semiconductor** apparatus such as **thin film transistors** (**TFT**) and MOS transistors, and also displays and electrooptic apparatus, such as image sensors.

ADVANTAGE - Improved interface between an active layer, particularly a channel forming layer, and a base film to improve ,e.g., **TFT** characteristics. High reliability of **semiconductor device**.

DESCRIPTION OF DRAWING(S) - The device shows the construction of a **semiconductor** apparatus (liquid crystal display).

Glass substrate (500)
Pixel matrix circuit (501)
Scan line **drive circuit** (502)
Signal line **drive circuit** (503)
Flexible printed circuit (510)
IC chip (511, 512)
Logic circuit (520)
Counter substrate (530)

61/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013013281
WPI Acc No: 2000-185132/200017
Related WPI Acc No: 1995-202132; 1996-430739
XRAM Acc No: C00-058210
XRPX Acc No: N00-136754

Manufacture of **thin film transistors** for liquid crystal device, comprises crystalline silicon **semiconductor** layer which has been heat crystallized at a relatively low temperature because of the use of a crystallisation promoting material

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: MIYANAGA A; OHTANI H; TAKEYAMA J

Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 984317	A2	20000308	EP 94308974	A	19941202	200017	B
			EP 99121017	A	19941202		

Priority Applications (No Type Date): JP 93339397 A 19931202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 984317	A2	E	23	G02F-001/1368	Div ex application EP 94308974 Div ex patent EP 656644

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 984317 A2
Abstract (Basic):

NOVELTY - An active matrix display device comprises a crystalline silicon **semiconductor** layer which has been heat crystallized at a relatively low temperature because of the use of a crystallisation promoting material such as Ni, Pd, Pt, Cu, Ag, Au, In, Sn, Pb, P, As, And Sb. This material is introduced by mixing it within a liquid precursor material for forming **silicon oxide** and coating the precursor material onto the amorphous silicon film.

DETAILED DESCRIPTION - An active matrix display device comprises:

(a) a **semiconductor** layer with first and second impurity regions and a channel formation region formed on an insulating surface;

(b) a gate **insulating film** adjacent the channel formation region;

(c) a gate electrode adjacent the gate **insulating film**;

(d) an **insulating film** (215) comprising an organic resin formed over the previous layers;

(e) a pixel electrode (216) formed on the **insulating film** and electrically connected to one of the first and second impurity regions; and

(f) a conductive **layer** formed on the **insulating film** and electrically connected to the other one of the first and second impurity regions.

An INDEPENDENT CLAIM is also included for an active matrix display

device comprising a glass substrate, a blocking film and a similar structure as above.

Preferably, the display device is a liquid crystal device.

USE - Manufacture of **thin film transistors** for integrated circuits, e.g. as switching elements in an active **matrix circuit** in an electro-optical device or as a **driving circuit** formed on the same substrate as the active **matrix circuit**.

ADVANTAGE - The concentration of catalyst for promoting the crystallisation can be accurately controlled and minimized.

DESCRIPTION OF DRAWING(S) - The drawing illustrates a process step for manufacturing a **thin film transistor** according to the invention.

Interlayer **insulating film** (214)
Transparent polyimide film (215)
Pixel electrode (216)
Electrode/wirings (217,218)
pp; 23 DwgNo 6F/8

61/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010037281
WPI Acc No: 1994-304992/199438
XRAM Acc No: C94-138995
XRPX Acc No: N94-239841
Thin film transistor mfr. - using three or four mask levels, esp. for flat LCD screen prodn
Patent Assignee: THOMSON-LCD (CSFC)
Inventor: HEPP B; SANSON E; SZYDLO N
Number of Countries: 019 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2702882	A1	19940923	FR 933012	A	19930316	199438	B
WO 9421102	A2	19940929	WO 94FR278	A	19940315	199439	
EP 689721	A1	19960103	EP 94909965	A	19940315	199606	
			WO 94FR278	A	19940315		
WO 9421102	A3	19941110	WO 94FR278	A	19940315	199610	
JP 9506738	W	19970630	JP 94520709	A	19940315	199736	
			WO 94FR278	A	19940315		
US 5830785	A	19981103	WO 94FR278	A	19940315	199851	
			US 96522243	A	19960222		

Priority Applications (No Type Date): FR 933012 A 19930316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2702882	A1		26	H01L-021/336	
WO 9421102	A2	F	24	H01L-021/00	
Designated States (National): JP KR US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 689721	A1	F		H01L-027/12	Based on patent WO 9421102
Designated States (Regional): DE FR GB NL					
JP 9506738	W		29	H01L-029/786	Based on patent WO 9421102
US 5830785	A			H01L-021/00	Based on patent WO 9421102
WO 9421102	A3			H01L-021/336	

Abstract (Basic): FR 2702882 A

A mfg. process for direct staged (gate above source and drain) TFTs with four mask levels involves (a) depositing and etching a first conductor level on an insulating substrate to form a source (1) and drain (2); (b) depositing and etching a **semiconductor** level alone or followed by a **first insulation** level joining the source and drain; (c) depositing and etching a **second insulation** level; and (d) depositing and etching a second conductor level (15) to form the gate of the transistor (20).

A similar process with three mask levels involves carrying out step (a); depositing a **semiconductor** level and an insulation level and etching both levels joining the source and drain; oxidising, nitriding or passivating the **semiconductor** level sidewalls; and depositing and etching a conductor level (15).

Also claimed are (i) a liq. crystal screen including an active

matrix, the **pixel electrode-driving** active elements of which are TFTs made by the above processes; (ii) a liq. crystal screen including an active matrix and an integrated driver, the active elements **driving** the pixel **electrodes** and forming the integrated driver being TFTs.made by the above processes; and (iii) an electronic circuit on an insulating substrate, made by the above processes.

The substrate is pref. a glass sheet. The conductive materials are Al, Ti, Cr, Mo, W, Ta, ITO, alloys or multilayers, the first conductive level pref. being of transparent ITO or SnO2. The **semiconductor** is a-Si:H, polysilicon or microcrystalline Si. The insulating material is **silicon dioxide**, **nitride** or **oxynitride**.

USE - In mfr. of flat LCD screens, esp. with integrated drivers.

ADVANTAGE - The processes allow passivation of the transistors during mfr., to make them insensitive to light from above, and allow connection of the gate of one transistor to the source or drain of the same or another transistor.

61/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06796720

MANUFACTURE OF **SEMICONDUCTOR DEVICE**

PUB. NO.: 2001-024201 [JP 2001024201 A]
PUBLISHED: January 26, 2001 (20010126)
INVENTOR(s): TAKEMURA YASUHIKO
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD
APPL. NO.: 2000-182149 [JP 2000182149]
Division of 05-186891 [JP 93186891]
FILED: June 30, 1993 (19930630)
PRIORITY: 04-207437 [JP 92207437], JP (Japan), July 10, 1992 (19920710)

ABSTRACT

PROBLEM TO BE SOLVED: To form a **TFT** having a large OFF resistance, in an active matrix region by a method wherein only a peripheral circuit part is masked, an anodic oxide in a matrix part is removed and the anodic oxide is formed uniformly on the surface and the side face.

SOLUTION: An anodic oxide is etched, and a metal aluminum film 106 is then etched. In addition, a peripheral circuit region is masked, an anodic oxide on a gate **electrode** in a **matrix** is etched, gate **electrodes** 108, 109 in a peripheral **drive circuit** part are formed, and a gate **electrode** 110 in a **matrix circuit** is formed. After that, a current is supplied only to the gate electrode 110, and an anodic oxide 111 is formed on the surface and the side face of the gate electrode 110. After that, an N-type region 112 and a P-type region 113 are formed in the peripheral circuit region, and a P-type region is formed in the **matrix circuit**. After that, a **silicon oxide film** as an interlayer **insulator** 115 is formed on the whole face. Lastly, an ITO film is etched, a pixel electrode 116 is formed, and chrominum interconnections 117 to 121 are formed.

61/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05004807
SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 07-297407 [JP 7297407 A]
PUBLISHED: November 10, 1995 (19951110)
INVENTOR(s): KOYAMA JUN
KAWASAKI YUJI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-107575 [JP 94107575]
FILED: April 22, 1994 (19940422)

ABSTRACT

PURPOSE: To provide a **semiconductor** integrated circuit having an excellent circuit characteristic by using P-channel TFTs for all monolithic active **matrix circuits** and an offset gate type **TFT** for the **TFT** constituting an active **matrix circuit**.

CONSTITUTION: Island-like areas 103-105 are formed by etching a crystallized silicon film. The areas 103 and 104 are used for TFTs constituting peripheral **drive circuits** and the area 105 is used for a **TFT** forming an active **matrix circuit**. Then a gate **insulating film** is formed by depositing a **silicon oxide** film 106. In addition, gate electrodes 107-109 are formed by depositing and etching an aluminum film. Offsets can be formed by satisfactorily utilizing an increased amount resulting from anodic oxidation when films 110-112 composed of a product of anodic oxidation are formed on the side and upper surfaces of the gate electrodes 107-109 by applying a voltage across the electrodes 107-109 in an electrolyte. Therefore, a **semiconductor** integrated circuit having an excellent circuit characteristic can be obtained, because the drain current of the circuit can be prevented from becoming large when a reverse bias current is supplied to the gate electrodes.

61/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01691761
CONSTITUTING METHOD OF **THIN-FILM TRANSISTOR**

PUB. NO.: 60-170261 [JP 60170261 A]
PUBLISHED: September 03, 1985 (19850903)
INVENTOR(s): YANAI KENICHI
KAWAI SATORU
NASU YASUHIRO
INOUE ATSUSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-025383 [JP 8425383]
FILED: February 14, 1984 (19840214)
JOURNAL: Section: E, Section No. 372, Vol. 10, No. 5, Pg. 132, January 10, 1986 (19860110)

ABSTRACT

PURPOSE: To etch hydrogenated amorphous silicon selective and easily, and to obtain electric connection to an ITO film stably at a low stepped section by forming a gate **insulating film** in the double layer constitution of an silicon nitride film and a **silicon oxide** film.

CONSTITUTION: An n(sup +) amorphous silicon film 7 forming an ohmic-contact to an operating **semiconductor** layer 5 and further source-drain electrodes 8 having the composition of NiCr are evaporated, and a resist pattern 6 is removed through a lift-off method, thus forming source-drain electrode sections. A resist pattern is shaped by using a mask, metallic electrodes for the source-drain electrodes 8 and the n(sup +) amorphous silicon film 7 are removed through etching, and a source electrode section and a drain electrode section are isolated while the hydrogenated amorphous silicon film 5 is removed through dry etching. Only the hydrogenated amorphous silicon silm 5 is removed selectively because the etching rate of a **silicon oxide** is very slow at that time. A display electrode 9 consisting of an ITO film is formed through the lift-off method, and a **matrix-driven** conductive film **circuit** is sh

63/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013152896
WPI Acc No: 2000-324768/200028
Related WPI Acc No: 1995-189149; 2000-324767; 2001-448065
XRPX Acc No: N00-244439
Drive circuit for active **matrix** LCD device, image sensor has areas having low **concentration impurity** in one of **thin film transistors** to overlap with its gate electrode
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000101095	A	20000407	JP 93269778	A	19931001	200028	B
			JP 99286129	A	19931001		

Priority Applications (No Type Date): JP 93269778 A 19931001; JP 99286129 A 19931001
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000101095	A		13	H01L-029/786	Div ex application JP 93269778

Abstract (Basic): JP 2000101095 A
Abstract (Basic):

NOVELTY - The **semiconductor** film formed below the gate **insulating film** has channel formation area across which two primary areas containing impurity of one conductivity are formed. Two secondary areas including **impurity** of low **concentration** than that of the primary areas are formed across the channel formation area. The secondary areas of one of the transistor overlap with its gate electrode.

DETAILED DESCRIPTION - Two **thin film transistors** formed on a substrate are provided with a gate electrode (105) formed on a gate **insulating film** (104) respectively.

USE - For active matrix LCD device, image sensor or three dimensional integrated circuit.

ADVANTAGE - Improves yield and uniform characteristics of **TFT**, by suppressing hot carrier effect.

DESCRIPTION OF DRAWING(S) - The figure shows production procedure of **TFT**.

pp; 13 DwgNo 7/8

63/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009483494
WPI Acc No: 1993-177029/199322
XRPX Acc No: N93-135676
Thin film transistor device for **driving** and **matrix circuit** - sets **impurity concentration** of low level **impurity** source and drain regions of peripheral circuit to first value, low **concentration impurity** source and drain regions of **matrix circuit** set to second value
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: MATSUMOTO H
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 544229	A1	19930602	EP 92119988	A	19921124	199322	B
JP 5142577	A	19930611	JP 91334597	A	19911125	199328	
US 5323042	A	19940621	US 92975852	A	19921113	199424	
EP 544229	B1	19980722	EP 92119988	A	19921124	199833	
DE 69226334	E	19980827	DE 626334	A	19921124	199840	
			EP 92119988	A	19921124		
KR 9702119	B1	19970222	KR 9220679	A	19921105	199934	

Priority Applications (No Type Date): JP 91334597 A 19911125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 544229	A1	E	9	H01L-027/12	
Designated States (Regional): DE FR GB					
US 5323042	A		8	H01L-027/01	
EP 544229	B1	E		H01L-027/12	
Designated States (Regional): DE FR GB					
DE 69226334	E			H01L-027/12	Based on patent EP 544229
JP 5142577	A			G02F-001/136	
KR 9702119	B1			H01L-027/12	

Abstract (Basic): EP 544229 A
The **thin film transistor** device has a first **thin film transistor** (14) with a **semiconductor** layer (22) and a source and drain regions coupled to ends of the channel region (22a) with a low level impurity region (22b), and a high level impurity region (22c), a gate **insulating film** (24), a gate electrode (26) and source drain electrodes (31 and 32).
A second **thin film transistor** (12) has **semiconductor** layer (21) with channel region (21a), source and drain regions coupled to ends of it, with both low and high level impurity regions (21b and 21c), gate **insulating film** (24), gate electrode (25), and source and drain electrodes (31 and 32). The impurities existing in the first and in the second transistor have same conductive type, and **concentration** of low level **impurity** region of first is set to be higher than that of the second.
ADVANTAGE - Forms **matrix circuit** and peripheral **driving circuits** where number of **thin film**

transistors can be considerably increased, with on current increase, and off current decrease.

Dwg.1/4

Abstract (Equivalent): US 5323042 A

In the case of an LDD-structure **thin film transistor**, an on-current becomes large as **impurity concentration** of low level **impurity** source and drain regions is increased. Then, when the **impurity concentration** is increased to a first **impurity concentration**, the on-current reaches to a substantially maximum point.

On the other hand, a cut-off current Ioff becomes substantially minimum when the **impurity concentration** is decreased to a second **impurity concentration**. The cut-off current is gradually increased even if the **impurity concentration** becomes higher or lower than the second **impurity concentration**. Therefore, **impurity concentration** of low level **impurity** source and drain regions of a **thin film transistor** for a peripheral circuit is set to a first **impurity concentration**, and that of low **concentration impurity** source and drain regions of a **thin film transistor** for a **matrix circuit** is set to a second **impurity concentration**.

ADVANTAGE - On-current can be increased, cut-off current can be reduced.

65/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012754301
WPI Acc No: 1999-560418/199947
XRAM Acc No: C99-163272
XRPX Acc No: N99-413982
Liquid crystal display apparatus for portable computers
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: AKIYAMA M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5952991	A	19990914	US 96748897	A	19961114	199947	B

Priority Applications (No Type Date): US 96748897 A 19961114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5952991	A		26	G09G-003/36	

Abstract (Basic): US 5952991 A
Abstract (Basic):
NOVELTY - Since the liquid crystal display of the invention comprises a number of voltage applying means (including **drive circuits**) for **driving** the liquid crystal, and a controlling means for switching the voltage means from one to another, the controlling means having the switched state, a number of display modes can be selected. With a display mode having a **low** driving frequency the **power** consumption is markedly reduced. In the display mode a gradation driving mode with high picture quality can be selected.

DETAILED DESCRIPTION - (A) Liquid crystal display apparatus comprising; (i) Means of applying a first voltage at a first frequency to a liquid crystal and having at least one nonlinear switching element and intersecting a scanning line so as to form a matrix. (ii) Means of applying a second voltage at a second and lower frequency to a liquid crystal and having at least one nonlinear switching element. (iii) Means for controlling the voltage alternately and having a memory portion for storing a switched state for switching between a sampling and a selected state, where the sampling state samples the first voltage at a sampling time and consequently applies a sampling voltage corresponding to the first voltage to the liquid crystal, and the selected state selects the second voltage. INDEPENDENT CLAIM - (B) Also included is the display as (A) in which the **matrix** is a **matrix** of **pixels electrodes** each having first, second, and memory portions, and first and second signal lines supply voltage to the pixels. A number of scanning lines intersect the first signal line. The first circuit samples a the first voltage and applies it to the pixel electrode, the second circuit is connected to the second signal line and the memory portion, selects a voltage applied to the second signal line and applies it to the pixel electrode. The memory portion stores a switched state by a signal supplied from the first circuit and switches alternately between a sampling state and a

selected state.
USE - Active matrix liquid crystal displays for portable computers etc.
ADVANTAGE - The apparatus has a marked reduction in power consumption of the **drive circuit** without affecting display quality.
DESCRIPTION OF DRAWING(S) - The drawing shows a pixel of a liquid crystal display.
pp; 26 DwgNo 1A/22

67/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04068191 INSPEC Abstract Number: B9202-7260-045
Title: A study of poly-Si **TFT** LCD with very small pixel size and high aperture ratio
Author(s): Shimada, T.; Ueda, T.; Takafuji, Y.; Komiya, H.
Author Affiliation: LCD Group, Sharp Corp., Nara, Japan
Conference Title: Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials p.641-3
Publisher: Bus. Center Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1991 Country of Publication: Japan xvi+770 pp.
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE; Inst. Electron. Inf. Commun. Eng. Japan; et al
Conference Date: 27-29 Aug. 1991 Conference Location: Yokohama, Japan
Language: English
Abstract: Active **matrix** LCD with very small **pixel** size is discussed. A technique of making **storage capacitor dielectric film** thinner than **TFT** gate **dielectric film** is proposed to reduce the area of **storage capacitor**. This technique is applied to the fabrication of test panels with 37 mu m*32 mu m pixel size, using HTO film as gate and **storage capacitor** dielectric. Poly-Si TFTs with LDD structure are used as switching devices to reduce off-current. Drivers are fully integrated with CMOS configuration. Aperture ratio is 32%, and contrast ratio more than 50:1 is obtained.